Project II.2: MATERIALS AND DEVICES FOR MEMORY APPLICATIONS

Project leader: P.Normand

Key researchers: V. Ioannou-Sougleridis, P. Dimitrakis

Collaborating Researchers: P. Argitis, N. Glezos, D. Davazoglou, A.M. Douvas

Post-doctorals: E. Makarona, D. Velessiotis

PhD candidate: P. Goupidenis, N. Nikolaou

Objectives

- Development of functional dielectrics and nanostructured materials for inorganic/organic memory applications.
- Study of the structural and electrical properties of the generated materials and demonstration of material functionality enabling the development of low-voltage memory devices.
- Realization and testing of memory devices and manufacturability assessment of the developed fabrication routes in an industrial environment.

Funding

- ESA - Sub-Contract FORTH-NCSRD- RFQ No 3-12083, 14/4/2008-14/4/2009

Activities

Our research activities in materials and structures for memory applications started in 1996 with the development of the low-energy ion-beam-synthesis (LE-IBS) technique in collaboration with Salford University (UK). Two-dimensional arrays of Si nanocrystals in thin gate dielectrics were demonstrated and further exploited in the fabrication of nanocrystal memories (NCMs). This activity was first supported by the EU project, FASEM (1997-2000). LE-IBS development with target the realization of non-volatile NCMs in an industrial environment has been conducted further within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer, Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last few years to novel NCMs alternatives including: (a) Memory devices by Si^+ irradiation through poly-Si/SiO_2 gate stack (Collaborators –Clrs-: FZR and ZMD AG both sited in Dresden (DE)), (b) Memory devices using Ge-NCs produced by MBE (Clr: Aarhus Univ. (DK)), (c) hybrid silicon-organic and SiGe-organic memories (Clr: Durham Univ. (UK)); this last activity was conducted within the framework of the EU project, FRACTURE (2001-2003), (d) Formation of Si NCs in thin SiO_2 layers by Plasma Immersion (Clrs: CEMES/CNRS, Ion-Beam-Services (IBS, FR)), (e) Wet oxidation of silicon nitride implanted with low-energy Si ions for ONO memory stacks (Clrs: CEMES/CNRS, MDM-INFM (IT)), (f) MOS structures with low-energy Ge-implanted thin gate oxides (Clr: LETI/CEA (FR)), (g) Proton radiation tolerance of nanocrystal memories (Clr: NTUA (GR)), (h) Fabrication and characterization of SiO_2 films with Si NCs obtained by stencil-masked LE-IBS (Clrs: CEMES/CNRS and INSA Toulouse (FR)), (i) Fluorene-based cross-bar organic memory device (Clrs: NTUA and Durham Univ.)

In 2009, our main activities described hereafter were focused on the following tasks: (A) Molecular storage elements for proton memory devices (Clrs: IMEL's projects I.2 & II.3, TEI Crete, Ioannina Univ.), (B) Formation of Ge nanocrystals in high-k dielectric layers for memory applications formation (Clrs: CEMES/CNRS, FZR Dresden, Cambridge NanoTech (USA)), (C) High-k dielectrics stacks for advanced non-volatile memory devices (Clrs: Helsinki Univ. (FI), IMS/NCSR'D'), (D) III-Nitrides quantum dots-resonant tunneling diodes as tunable wavelength UV-VIS phototodetectors (Clr: MRG/FORTH (GR)), (E) Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride (Clr: CEMES/CNRS), (F) Hybrid organic thin film transistor by laser-induced-forward-transfer (Clrs: NTUA, IMS/NCSR'D), (G) Fabrication and characterization of Ge diodes (Clr: IMS/NCSR'D').

MAIN RESULTS IN 2009

A. Molecular storage elements for proton memory devices

E. Kapetanakis[1], A.M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Dimitrakis, K. Beltsios[2], P. Goupidenis, P. Normand

**Assistant Professor at the Department of Electronics, TEI Crete*
*** Assistant Professor at the Department of Materials Science Engineering, University of Ioannina*

We recently demonstrated the concept of bi-functional molecular ionic dielectric stacks combining ion transport with ion trapping/detrapping functions for the further development of reprogrammable non-volatile single-OFET memory devices (see Kapetanakis et al. Adv. Mater. 20, 4568, 2008). The information carriers were in the form of protons and the dielectric stacks consisted of a proton-conducting layer (PCL) and a proton-trapping layer (PTL). The PCL was a poly(methyl methacrylate) (PMMA) film with embedded molecules of 12-tungstophosphoric acid ($H_3PW_{12}O_{40}$), while the PTL was a PMMA film containing 2-aminoanthracene molecules.

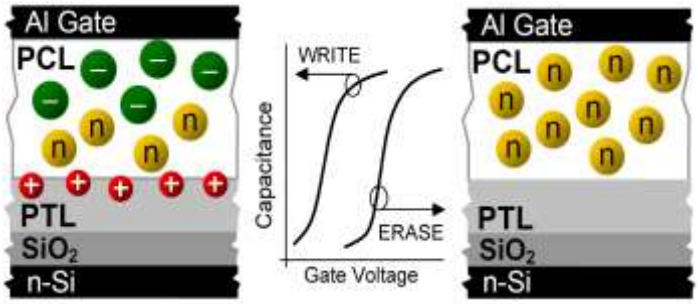

Fig. 1: *Schematic illustrating the structure and the operation principle of a non-volatile bistable MIS memory device with a molecular-based proton storage element consisting of a PCL / PTL stacked structure.*

The concept of using a PCL/PTL-type stack for the realization of non-volatile proton memory devices is quite simple (see figure 1) and many materials are possible candidates. The materials' selection is primarily guided by requirements of memory performance and process compatibility that strongly depend on the physicochemical properties of the candidate materials. This year, we focused our efforts on the optimization of the thermal processing parameters (temperature and duration) used in preparation of the above PCL-PTL materials. FTIR investigations resulted in the successful prevention of two undesirable phenomena for the device stability and performance: (a) the reaction between HPW and PMMA matrix inside the PCL, and (b) the intermixing of the PCL and PTL layers (see Kapetanakis et al., organic electronics 10, 711, 2009).

Moreover, a combination of UV spectroscopy studies and transient current (TC) experiments on MIS structures provided a comprehensive picture about the protons involved in the memory effect and their motion through the PCL. The concentration of the HPW molecules within the PCL was estimated to approximately 1.9×10^{20} HPW molecules cm^{-3} while a proton density of ~3.8×10^{17} protons/cm^3 was extracted from TC measurements under full polarization conditions, indicating that the main part of the dissociated protons which are attached to polymer basic sites is mainly immobile.

Finally, the material features of a generic PCL/PTL stacked structure, which affect the operation of a molecular proton memory device, were examined from a theoretical point of view. Results indicate that the write characteristics of this type of memory such as the magnitude of the memory window and the write speed depend on the thickness, the proton mobility and the proton concentration of the PCL, while the write voltage is mainly determined by the thickness of the PTL. In light of these analyses, it appears that memory windows as large as 2.8V might be obtained for a 1ms / 3V write operation regime even in the case of relatively thick PCL/PTL. These observations suggest that a PTL/PCL storage element is appealing for low-cost low-power non-volatile single-OFET memory applications.

Our next research activities include the development of organic/inorganic single-FET memory devices using the above PTL/PCL stacks and advanced electrical characterization of the polarization / depolarization mechanisms taking place in the PCL.

B. Formation of Ge nanocrystals in high-k dielectric layers for memory applications

P. Dimitrakis, V. Ioannou-Sougleridis, P. Normand, C. Bonafos[1], S. Schamm[1], A. Mouti[1], B. Schmidt[2], J. Becker[3]

[1]CEMES-CNRS, Université de Toulouse, Toulouse, France
[2]Research Center Dresden-Rossendorf, Dresden, Germany
*[3]Cambridge Nanotech Inc, Cambridge, MA, USA**

Semiconductor nanocrystals (NCs) have been employed successfully in various demonstrators for new CMOS device applications like nonvolatile memory (NVM) cells and optoelectronic components. Ge NCs are of special interest for nano-floating gate NVM cells due to their negative conduction band offset with respect to the Si substrate conduction band; an attractive NC property for faster programming speeds and longer retention times compared to silicon NCs. Another interesting option is the use of high-k materials as tunneling dielectrics. This route has been examined to overcome the charge retention issues rising from the thinning of the injection SiO_2 layer. Based on the above, Ge-NCs embedded in high-k dielectrics provide a promising alternative in the development of NC-NVM.

In previous studies (see 2006 IMEL annual report), formation of Ge-NCs into Al_2O_3 thin layers by low-energy Ge implantation and subsequent furnace annealing at 800°C was demonstrated. In the present work, 5nm-thick Al_2O_3 and 7nm-thick HfO_2 layers were grown by ALD on Si substrates and subjected to 1keV Ge+ implantation at doses of 0.5 or $1x10^{16}$ cm^{-2}. After deposition of a 10nm-thick Al_2O_3 (or HfO_2) layer, different furnace annealing steps in N_2 ambient were carried out to examine in a more comprehensive way the effect of the annealing temperature on the structural and electrical properties of the implanted high-k materials.

TEM and Electron Energy Loss Spectroscopy (EELS) studies revealed the presence of Ge-NCs only in the annealed Al_2O_3 layers (see Fig.2). These NCs have a mean diameter of 5nm and are located at a tunneling distance of 1 to 3 nm from the Si substrate. Further analysis revealed the presence of 1 nm thick SiO_2 layer at the Al_2O_3/Si substrate interface as well as crystallization of the alumina matrix. Capacitance-to-voltage (C-V) measurements performed on Al-gate MIS capacitor structures at various test ac-signal frequencies exhibited hysteresis due to charge storage in implantation-induced-defects and NCs. In the case of the $10^{16}cm^{-2}$ implanted samples, an annealing temperature in the 800 – 950°C range defines a safe process window, i.e., without significant changes in the memory window (see Fig. 3). The reduction of memory window observed at 1050°C might be related with Ge out-diffusion and dissolution of very small Ge clusters. Current-to-voltage (I-V) characteristics suggest that the higher the temperature of post-implantation annealing the lower the conduction through the Al_2O_3 layer especially at low electric fields. Retention performance of the above samples is under investigation.

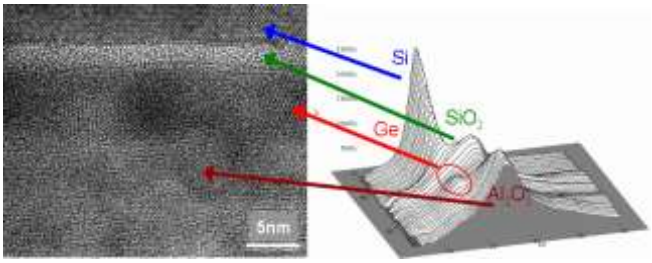

***Fig. 2**: XTEM and EELS analysis of Al_2O_3 thin film implanted with 10^{16} Ge^+ cm^{-2} and annealed at 800°C.*

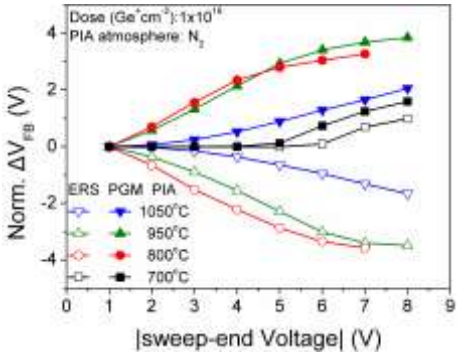

***Fig. 3**: Memory windows obtained from C-V hysteresis using MIS capacitors with Al_2O_3 gate insulator implanted with Ge and annealed in N_2 at different temperatures.*

C. High-k dielectrics stacks for advanced non-volatile memory devices

N. Nikolaou, V. Ioannou-Sougleridis, P. Dimitrakis, K. Giannakopoulos[1], P. Normand, K. Kukli[2], J. Niinisto[2], M. Ritala[2], M. Leskela[2]

[1]Institute of Materials Science, IMS-NCSR "D"
[2]Chemical Department of Helsinki University (FI)

The objective of this project is to examine the influence of advanced atomic layer deposition (ALD) precursor chemistry of high-k dielectrics, used as tunnel or control insulators of nitride-based memory structures, in order to improve the functionality and performance of SONOS-type devices. This project is conducted in close collaboration with the University of Helsinki.

Silicon nitride-based charge trapping memories are being considered as a promising alternative which could alleviate the serious downscaling limitations of the conventional flash memories. However, the most prominent issue of the latter devices is the inability to reduce further the vertical dimensions of the memory stack and at the same time to satisfy the 10-years retention requirement. In turn, the silicon nitride charge trapping devices must resolve a number of drawbacks and in particular the "over-erase"-saturation effect. This can be accomplished by the replacement of the standard SiO_2 tunnel and control oxides by high-k dielectrics layers. It is evident that the ALD precursor chemistry becomes gradually the critical factor which determines the physical, chemical and electrical properties of the deposited high-k dielectrics.

During the last year the main activity was focused on the examination of the structural and electrical properties of $SiO_2/Si_3N_4/ZrO_2$ or $SiO_2/Si_3N_4/HfO_2$ gate stacks with layer thicknesses of 2.5/5/10 nm respectively. Both high-k layers were deposited using zirconium and hafnium alkylamide or cyclopentadielyl precursors in combination with ozone as the oxygen source.

In the case of the ZrO_2 gate stacks and independently of the used precursor, a memory window of about 6 V was achieved after application of ±10V/100ms pulses (see Fig.4). In addition to the charging behavior, no significant differences have been detected in the I-V and C-V characteristics between the ZrO_2 layers synthesized by the two different precursors. However, in terms of reliability the alkylamide precursors provide ZrO_2 layers with higher dielectric strength. In the case of HfO_2 blocking layers the memory window and the dielectric strength are significantly affected by the precursor. The alkylamide-formed- HfO_2 and the cyclopentadienyl-formed-HfO_2 show write windows of 9 and 7V, respectively. Moreover, it appears that the alkylamide precursor provides a HfO_2 layer with a higher dielectric strength. Pulsed operation reveals that HfO_2 based gate stacks exhibit reasonable charge trapping after the application of voltage pulses 11 V at 0.1 ms.

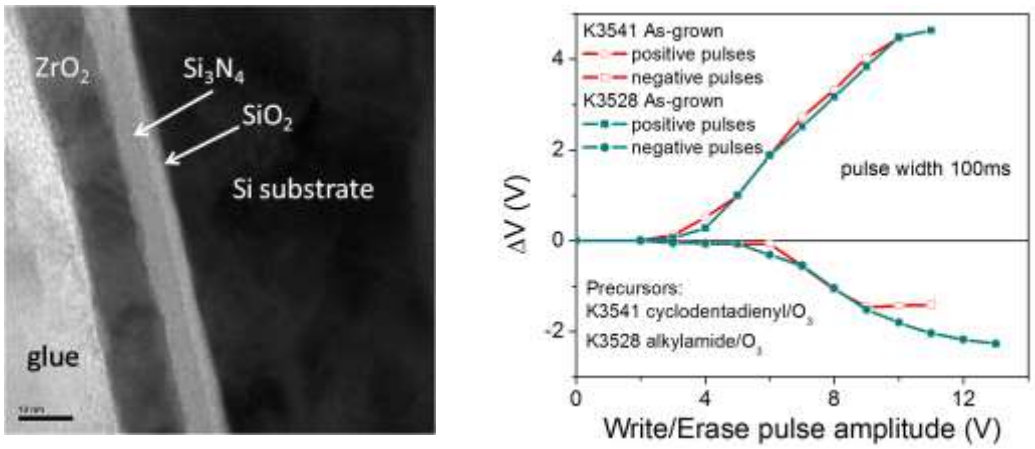

***Fig. 4**: (a) Transmission electron microscopy image of $SiO_2/Si_3N_4/ZrO_2$ gate stack on a silicon substrate where the ZrO_2 was deposited by the cyclopentadienyl precursor. (b) Flat-band voltage shift versus the amplitude of the applied write/erase pulse in the case of the $SiO_2/Si_3N_4/ZrO_2$ gate stack capacitors using alkylamide- or cyclopentadienyl-formed-ZrO_2.*

D. III-Nitrides quantum dots-resonant tunneling diodes as tunable wavelength UV-VIS phototodetectors

P. Dimitrakis, E. Iliopoulos[1], G. Deligiorgis[1], P. Normand, G. Konstantinidis[1], A. Georgakilas[1]

[1]Department of Physics & MRG/FORTH (GR)

The objective of these activities is to design, fabricate and evaluate the performance of a novel solid-state photodetector device with spectroscopic capability, operating in the ultraviolet-visible part of the electromagnetic spectrum. The proposed device principle combines the broad spectrum responsivity of a layer containing non-uniform size distribution of (In)GaN quantum dots (QDs) with energy selective read-out mechanism based on AlGaN/GaN asymmetric double quantum-well resonant tunneling diode (RTD) structures.

Clear evidence for the functionality of our RTD devices was presented last year (see 2008 IMEL annual report). However, these devices were suffering from large leakage currents and high density of surface states that cause screening of the NDR region and unexpected switching of current to high values. These experimental findings revealed the presence of two major issues in device fabrication: (a) the optimization of the insulating dielectric surrounding the diode structure and (b) the passivation of the diode surface before insulator's deposition. This year, we focused our efforts on these issues as well as on the growth conditions of GaN QDs for optimizing their structural characteristics.

More than twenty different single/double-well RTD structures were grown using MBE and more than five processing routes were applied for device fabrication. A case study is presented hereafter. Figure 5 shows XRD measurements on a single well RTD structure. The excellent agreement between the measurements and the fitted model reveals the high quality of the grown layers and their interfaces. Utilizing this structure, several devices were fabricated following four different processing routes for surface passivation. Next, a LPCVD TEOS SiO_2 layer was used for device isolation. The I-V characteristics of these devices are shown in figure 6. Obviously, the surface passivation process affects the leakage current of the diodes and the observation of the NDR phenomenon. Only devices realized following recipes B and C exhibit resonant tunneling due to the effective passivation of the surface states. Further investigations are currently in progress to optimize the peak-to-valley ratio in the I-V characteristics of the later devices.

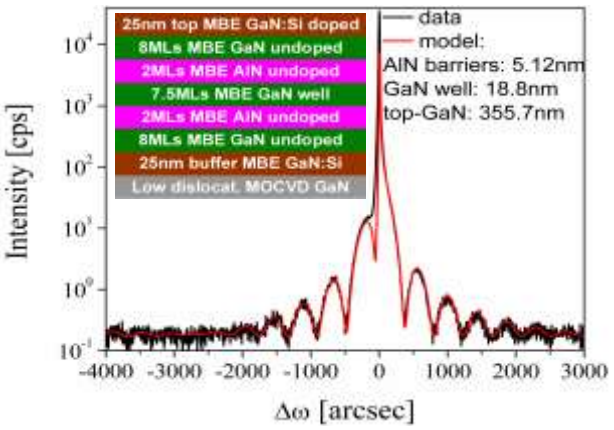

***Fig. 5**: (0002) ω-2θ scan XRD data of a single-well RTD structure (inset) and the corresponding dynamical theory simulation (red line).*

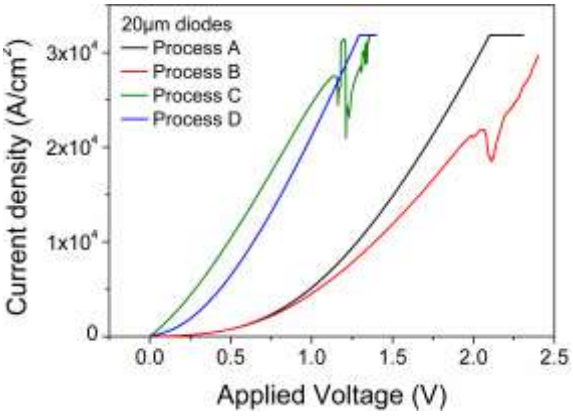

***Fig. 6**: I-V characteristics of the tested RTD devices fabricated following four different processing routes. The RTD structure is shown in Fig.5. Process B seems to be the most promising.*

E. Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride

N. Nikolaou, V. Ioannou-Sougleridis, P. Dimitrakis, P. Normand, S. Schamm[1], C. Bonafos[1], A. Mouti[1], G. BenAssayag[1]

[1]CEMES-CNRS, Université de Toulouse, Toulouse, France

Part of our last year efforts was devoted to the study of the physical phenomena that occur in memory structures consisting of $SiO_2/Si_3N_4/SiO_2$ gate stacks with silicon nanocrystals (Si-NCs) embedded within the silicon nitride material. The Si-NCs were synthesized by low-energy ion implantation into the silicon nitride layer followed by the deposition of a SiO_2 capping layer and subsequent annealing. At high Si implantation doses (1-1.5x10^{16} ions/cm^2) these structures exhibit clear current peaks followed by a negative differential resistance region, for both gate voltage polarities (see Fig.7a). Electrical examination was performed at temperatures from 20 to 100^{o}C using constant ramp-rate I-V measurements. This approach provides a valuable tool for the determination of the origin of the observed current peaks as well as to extract useful information about the trapping location of the injected charge within the dielectric stack. The formation of the current peaks is due to a displacement current (Fig. 7b) which develops during the transfer of charge carriers from the Si substrate to the Si-NCs. Analysis of the characteristics revealed that the carriers are trapped within the Si-NCs band, (Fig. 7c and 7d) verifying this region corresponds to energy minima of the dielectric stack (see Nikolaou et al., Nanotechnology 20, 2009).

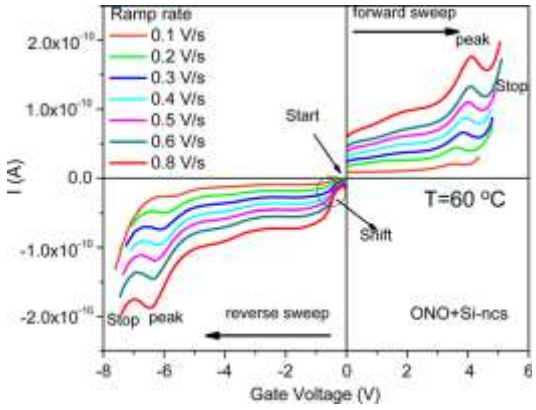

***Fig. 5a**: Constant ramp rate I-V characteristics of the implanted ONO structure showing the current peaks*

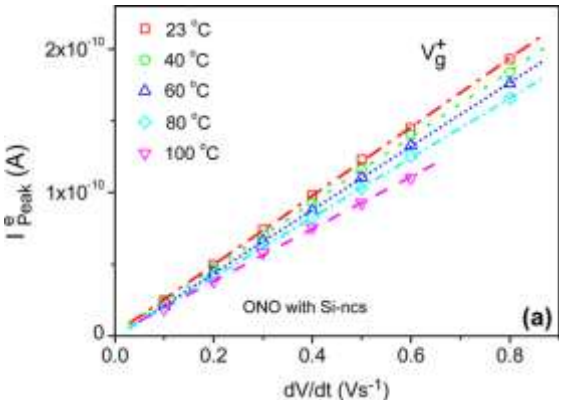

***Fig. 7b**: Electron current peak magnitude vs ramp rate. The linear relation indicates that the current peak is a displacement current.*

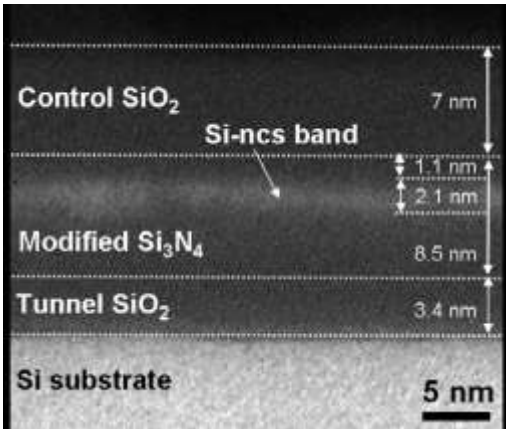

***Fig. 7c**: Cross section EFTEM image of the SiO_2/Si-Nc Si_3N_4/SiO_2 structures under study.*

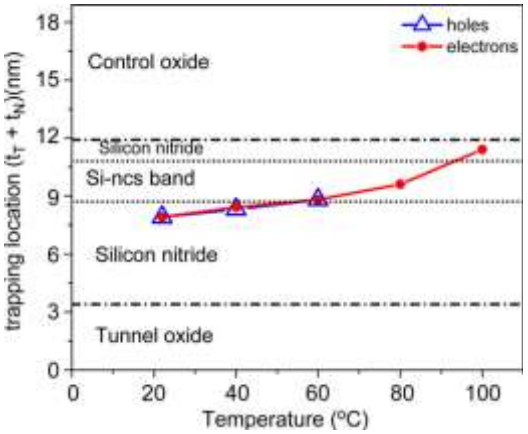

***Fig. 7d**: Variation of the trapping location of the injected carriers with temperature.*

F. Hybrid organic thin film transistor by laser-induced-forward-transfer (LIFT)

P. Dimitrakis, P. Normand, S. Chatzandroulis, M. Makriyianni[1], I. Zergioti[1], A. Speliotis[2]

[1]Department of Physics, School of Applied Sciences, NTUA (GR)
[2]Institute of Materials Science, IMS-NCSR "D"

The Laser Induced Forward Transfer (LIFT) technique is a promising alternative for maskless manufacturing of organic electronic components on flexible substrates when usual techniques, such as inkjet or roll-to-roll printing, cannot be used. Our research activities in this area were focused on the fabrication of organic thin-film transistors (OFETs) using solid phase LIFT semiconducting polymer material. The LIFT step carried-out at NTUA for the deposition of regioregular poly-3-hexylthiophene (P3HT) materials was successfully integrated to the device process flow developed at IMEL for bottom gate OFETs.

More specifically, a dry silicon dioxide layer 80-100nm thick was first grown on an implanted p-type Si substrate (receiver substrate) acting as the gate oxide and the gate electrode respectively. Au/Ti metal pads were sputtered (IMS) onto the SiO_2 layer through a shadow mask, forming the source and drain electrodes. Then, the polymer material (RR-P3HT) was transferred using the LIFT technique from a donor substrate (i.e., a quartz substrate with spin-coated P3HT materials) onto the receiver substrate placed in between the source and drain electrodes and covering partially the metal pads, as shown in figure 8. The distance between the S/D electrodes defines the gate length of the transistor which was about 100μm. Upon irradiation, the donor and the receiver substrates are located in close proximity. The resulting transistors were characterized at IMEL by parametric *I-V* measurements. It was found that the mobility of the P3HT layer is similar to that of conventional spin-coated P3HT. Furthermore, the source to drain current measurements under zero gate bias revealed that bulk conductivity of P3HT is due to a space-charge-limited-current mechanism. Figure 9 shows typical transfer characteristics, (i.e. I_{DS}-V_{GS}), at relatively low V_{DS}=-15V, of the tested OFETs from which a threshold voltage (V_T) around -20V has been extracted. Further investigations on the structural properties of the P3HT transferred layers and on the optimization of the transistor characteristics are in progress.

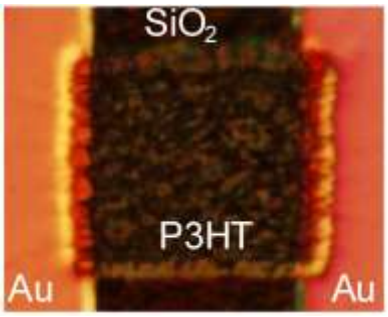

***Fig. 8**: Optical microscope image of a single P3HT layer printed using the LIFT technique on top of a SiO_2 layer and between the source/drain electrodes (Ti/Au).*

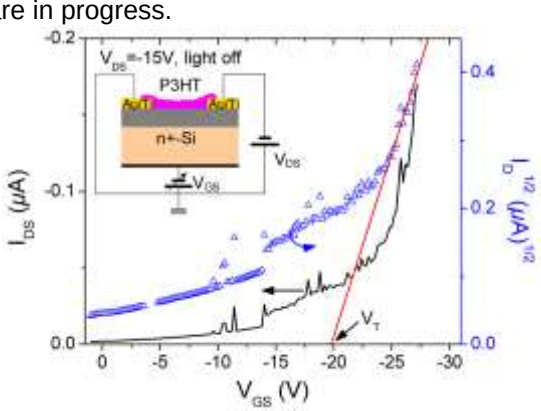

***Fig. 9**: Typical transfer characteristics of OFETs using LIFT-deposited-RR-P3HT materials.*

G. Fabrication and characterization of Ge diodes

V. Ioannou-Sougleridis, A. Golias*, A. Speliotis*, A. Dimoulas*

**Institute of Materials Science NCSR 'D'*

The objective of this research activity is the development of junction diodes on Ge substrates at temperatures lower than 400^{o}C. The severe scaling limitations of the conventional MOSFET fabricated on a Si substrate, and especially the limited drive current, require the replacement of the channel material. Germanium constitutes an attractive technological option due to the high mobility of both electrons (two times higher than Si) and holes (four times higher than Si). Although in terms of mobility, this material is ideally suited as channel material for high-performance logic applications, the germanium substrates integration technology faces significant challenges. A critical parameter is the formation of n+/p and p+/n junction diodes using low thermal budgets and low temperatures, a requirement to preserve the high-k dielectric integrity.

The diodes were formed by phosphorus or boron ion implantation using a dose of $2x10^{15}$ ions/cm^2. In order to facilitate low temperature dopant activation, a 50nm-thick Pt layer was deposited on the diodes, followed by a thermal annealing at 350^{o}C. During annealing Pt diffuses within germanium and Ge diffuses within the Pt layer. These parallel movements lead to the formation of a platinum-germanide layer. The extent of the PtGe reaction depends mainly on the type of the implanted dopant (phosphorus or boron) and the annealing conditions. During the platinum germanide formation, process dopant activation takes place. Figure 10a shows the I-V characteristics of an n+/p diode after annealing at 350^{o}C for time intervals between 2 and 30 min. Note the high drive current of 400 A/cm^2. The characteristics exhibit a maximum value of I_{on}/I_{off} ratio of $1x10^4$. At extended annealing the quality of the diodes degrades both in the forward and the reverse bias regimes. Figure 10b shows the I-V characteristics of a p+/n diodes fabricated by the same process. In this case an excellent value of I_{on}/I_{off} ratio of $1x10^5$. These characteristics of both n+/p and p+/n diodes reveal that the metal induced dopant activation process could resolve the issue of low temperature diode formation on germanium substrates

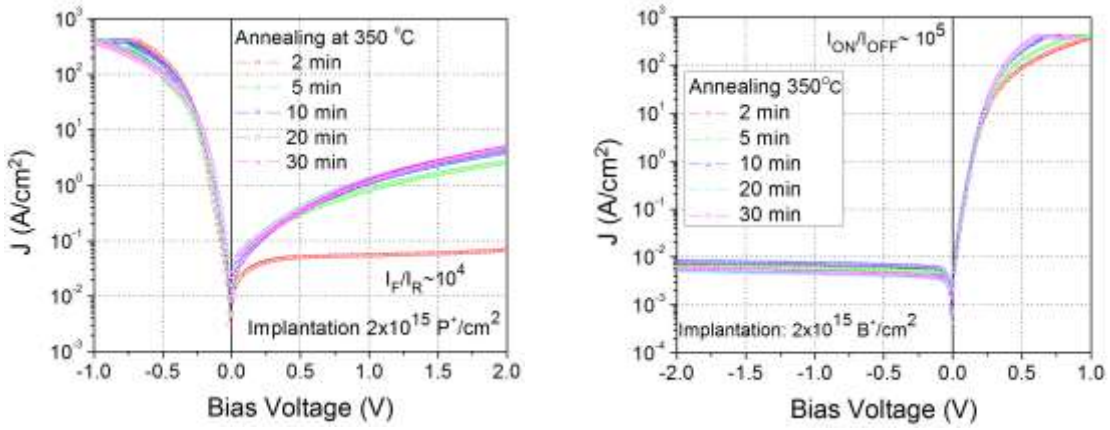

Fig. 10: *J-V characteristics of n^+/p (a) and p^+/n (b) Ge diodes as a function of annealing time at 350^{o}C. The diodes were fabricated by ion implantation, Pt deposition and annealing*.

PROJECT OUTPUT in 2009

Publications in International Journals

1. "Hybrid organic-inorganic materials for molecular proton memory devices", E. Kapetanakis, A.M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Normand, , Organic Electronics: physics, materials, applications 10, 711-718, 2009.
2. "Temperature-dependent low electric field charging of Si nanocrystals embedded within oxide-nitride-oxide dielectric stacks", N. Nikolaou, P. Dimitrakis, P. Normand, P., S. Schamm, C. Bonafos, G. Ben Assayag, A. Mouti, V. Ioannou-Sougleridis, Nanotechnology 20, Article number 305704, 2009.
3. "Ultra-low-energy ion-beam-synthesis of Ge nanocrystals in thin ALD Al2O3 layers for memory applications", P. Dimitrakis, A. Mouti, C. Bonafos, S. Schamm, G. Ben Assayag, V. Ioannou-Sougleridis, B. Schmidt, J. Becker, P. Normand, , Microelectronic Engineering 86, 1838-1841, 2009.
4. "Structured ZnO-based contacts deposited by non-reactive rf magnetron sputtering on ultra-thin SiO2/Si through a stencil mask", A. Barnabé, M. Lalanne, L. Presmanes, J.M. Soon, Ph. Tailhades, C. Dumas, J. Grisolia, A. Arbouet, V. Paillard, G. BenAssayag, M.A.F. van den Boogaart, V. Savu, J. Brugger, P. Normand, Thin Solid Films 518, 1044-1047, 2009.

Publications in International Conference Proceedings

1. "Memory Structures Based on the Self-organization of Cu Nanoparticles Deposited by Hot-Wire CVD on Polythiophene Layers", P. Dimitrakis, G. Papadimitropoulos, L. Palilis, M. Vasilopoulou, P. Normand, P. Argitis, and D. Davazoglou, ECS Trans. 25, 1073, 2009.
2. "Metal induced low temperature activation and La2O3 passivation of germanium n+/p and p+/n junctions", V. Ioannou-Sougleridis, A. Dimoulas, P. Tsipas and Th. Speliotis, proceedings of the 39th European Solid-State Device Research Conference (ESSDERC) September 14-18 Athens, Greece pp 367-370.

3. “Localized silicon nanocrystals fabricated by stencil masked low energy ion implantation: effect of the stencil aperture size on the implanted dose” R. Diaz, C. Dumas, J. Grisolia, T. Ondarçuhu, S. Schamm, A. Arbouet, V. Paillard, G. BenAssayag, P. Normand, J. Brugger, MRS Symp. Proc. 1160, pp. 61-66, 2009

Conference Presentations

1. “Memory Structures Based on the Self-organization of Cu Nanoparticles Deposited by Hot-Wire CVD on Polythiophene Layers”, P. Dimitrakis, G. Papadimitropoulos, L. Palilis, M. Vasilopoulou, P. Normand, P. Argitis, D. Davazoglou, , EUROCVD-17 and CVD-XVII, 216th Meeting of the Electrochemical Society, 4-9 October 2009, Vienna, Austria.
2. “Ultra-low-energy ion-beam-synthesis of Ge nanocrystals in thin ALD Al2O3 layers for memory applications”, P. Dimitrakis, A. Mouti, , C. Bonafos, S. Schamm G. Ben Assayag, V. Ioannou-Sougleridis, B. Schmidt, J. Becker, P. Normand, INFOS 2009, 29 June – 1 July, Cambridge, UK.
3. “Metal induced low temperature activation and La2O3 passivation of germanium n+/p and p+/n junctions”, V. Ioannou-Sougleridis, A. Dimoulas, E. Golias, Th. Speliotis, 39th ESSDERC, September 14-18, Athens, Greece.
4. “High Performance Germanium n+/p and p+/n Diodes Using Low Temperature Metal Induced Dopant Activation and La2O3 Passivation”, A. Dimoulas, P.Tsipas, Th. Speliotis, V. Ioannou-Sougleridis, 216th Electro-Chemical conference, October 4 - 9, 2009 , Vienna, Austria.

Invited Talks and Tutorial lectures

1. “Discrete charge storage memories”, P. Dimitrakis, Workshop on Nanoelectronics and Nanophotonics, Ankara, Turkey, January 26-28, 2009 (invited talk)
2. “Nanoparticle Memories: CMOS, Organic and hybrid approaches”, P.Dimitrakis, Winter School on Nanoelectronics and Nanophotonics, Bilkent University, Ankara, Turkey, January 20-25, 2009 (tutorial lecture)
3. “The Physics of Advanced and Emerging Flash Memories”, P. Dimitrakis, Sympos. H, Tutorial Notes, MRS Spring Meeting, 13-18April, San Francisco 2009 (Tutorial lecture)

Edition of Conference Proceedings

1. Proceedings of the 34th International Conference on Micro- and Nano-Engineering, MNE 2008, Athens, Greece, September 15-19, 2008, edited by I. Raptis, E. Gogolides, P. Normand and A. Tserepi., Microelectronic Engineering 86 (4-6), pp. 435-1518, April-June 2009.

Conference Organization

1. 39th European Solid-State Device Research Conference (ESSDERC), Athens, 14-18 September, 2009, Program co-Chair: P. Normand, Poster Session co-Chair: P. Dimitrakis.
2. Workshop “Nanotechnology for electronic and photonic applications”, Athens, 18 September, 2009

Patent

1. International patent application (PCT/GR2009/000023, 14/04/2009), Memory devices using proton-conducting polymeric materials, Inventors: E. Kapetanakis, A.M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Normand.