Project III. 3: THIN FILM DEVICES for LARGE AREA ELECTRONICS

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Objectives

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors (TFTs) fabricated in such films. Such advanced TFTs are necessary for next generation large area electronics systems, which are now in the research and development phase. Specifically, the targets of the project are:

- Evaluation of device parameter hot carrier and irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films with sequential lateral solidification (SLS).
- Investigation of the influence of the crystallization technique and the film thickness on TFT performance, defect densities and degradation for technology optimization.
- Investigation of effects of variations in TFT device structure and in the fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Assessment of material properties of ELA poly-Si TFTs using optical measurements.

Funding

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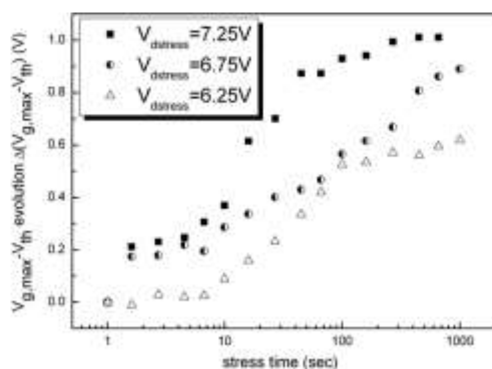
MAIN RESULTS IN 2009

A. Characterization of SLS ELA TFTs

Low temperature polycrystalline silicon thin film transistors are essential for large area electronics and high performance flat panel displays. In recent years, LTPS TFT performance has substantially increased due to important breakthroughs in the field of polycrystalline silicon crystallization and also due to the optimization of the process steps that differ from those of typical MOSFETs, mainly because of the requirement for low temperature procedures. The object of the present task was the electrical characterization of polycrystalline Silicon thin film transistors, crystallized with different variations of the advanced technique SLS ELA, and the determination of process technological parameters that affect the device performance, in order to further optimize the production of such high performance transistors.

We began studying the effect of the TFT active region film microstructure, relating the film characteristics themselves with the electrical performance and reliability characteristics of the TFTs. We found a new electrical characterization parameter ($V_{g,max}$-V_{th}), offering new insight on poly-Si trap density. This parameter proved especially useful in the understanding of degradation mechanisms under dc stress, allowing us to distinguish tail state generation (Fig. 1) from interface state generation (Fig. 2). We verified and probed the reasons for the superiority of the SLS ELA crystallization technique compared to SPC. Electrical characterization of TFTs crystallized with different SLS ELA techniques revealed specific relationships between microstructural characteristics and electrical ones.



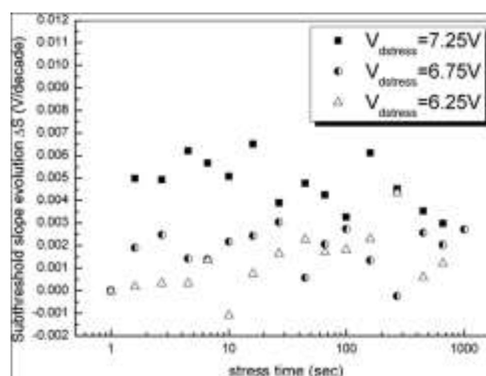


Fig. 1: Evolution of $V_{g,max}$–V_{th} (quantity proportional to the tail states density) with stress time for n-channel TFTs crystallized with the location control technique.

Fig. 2: Evolution of subthreshold slope S (quantity proportional to the interface states density) with stress time for n-channel TFTs crystallized with the location control technique.

Then, we examined the relationship between critical process steps and SLS ELA TFT performance. We found that the method of gate dielectric deposition significantly affects the TFT electrical parameters and also their degradation mechanisms. We also concluded that the doping and activation procedures could optimize the fabrication procedure, since a p- type doping could yield films with lower grain boundary trap densities. Channel dimensions should carefully be selected, since there are specific, technology related, narrow width and short channel mechanisms.

We also studied the role of the topology (top gate, bottom gate, double gate) on TFT performance. We observed that bottom gate structures are more likely to fail, due to the crystallization technique and the thickness of the films utilized. Even if they are operational, they will feature larger trap densities, due to the aforementioned reasons. A physically based model was developed for a double gate TFT with smaller bottom gate length than top one. The application of this model could give quantitative estimations of the oxide charge and interface trap densities.

Finally, we tried to modify the typical TFT fabrication procedure, studying the use of alternative gate dielectrics. We focused on the high-k dielectric HfO_2, fabricated capacitors using this material and studied possible, low temperature compatible gate electrodes. We concluded that the best possible gate electrode material to be used for LTPS HfO_2 TFT is tungsten (W).

To sum up, through the work within this task we extracted new characterization methodologies and new relationships between the electrical and technological characteristics of high performance LTPS TFTs, while at the same time suggesting specific optimization points for all of the critical steps in the fabrication procedure. Therefore, the work within this task is a useful tool-guide for an optimized fabrication procedure of high performance LTPS TFTs.

B. Modeling of hot carrier stress degradation mechanisms

Even though hot carrier phenomena have been widely studied in MOS poly-TFT structures, their quantitative impact in the reliability and performance characteristics of poly-TFT devices of different channel widths after electrical stressing under different stress conditions has been described only to a limited extent. Moreover, even in the models developed for the mature technologies of SOI (Silicon On Insulator) devices, typical bulk-MOSFETs and a-Si:H TFTs, the effect of subjecting devices with various channel widths under different hot carrier stress conditions has not been analyzed and mainly STI (Shallow Trench Isolation) PMOS devices have been investigated so far. Consequently, the effect of different hot carrier stressing conditions on the 1-D current-voltage characteristics as a function of the channel width needs to be further examined.

Thus, concerning the investigation of LTPS TFT degradation under DC stress, a practical model has been developed, with the key assumption being the formation of two channel regions, a defective and a non defective one. This is indicated in the schematic of Figure 3. The parameters that the model predicts are the mobility and the threshold voltage for the two regions and the extent ΔL of the degraded region. The equivalent circuit model of a device that has been subjected to electrical stress is represented by two TFTs connected in series.

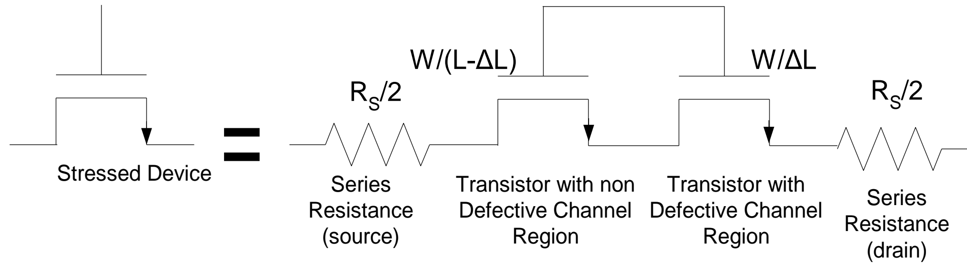


Fig 3: Schematic of TFT structure (left) and its equivalent electrical representation after electrical stressing (right). The developed model suggests the formation of two channel regions that are represented by two transistors connected in series.

In order to obtain a simple and practical expression, so as to predict the hot carrier damage for large grain size polysilicon TFTs, we use the on-current model proposed in an earlier work (Farmakis et al, IEEE Trans. Electron Dev. 2001; 48: 701-706):

Developing the mathematical formalism of the model and assuming monoenergetic traps at the grain boundaries, we eventually arrive at an expression for I_{DS} and subsequently for the total measured resistance R_{DS} (which is equal to the $R_A + R_B + R_S$, where the indices A (or nd) and B (or d) correspond to the undamaged and damaged areas and S to the source / drain contacts) as follows:

$$\frac{g_m V_{DS} C_{ox}}{I_{DS}^2} = \left[\frac{L}{W \mu_{0,nd} \left(V_{GS} - V_{th,nd}\right)^2} - \frac{\Delta L}{W \mu_{0,nd} \left(V_{GS} - V_{th,nd}\right)^2} + \frac{\Delta L}{W \mu_{0d} \left(V_{GS} - V_{th,d}\right)^2} \right]$$

which is the fitting function of the model.

The parameter ΔL is the most critical one for the stress experiments and the fitted data that were found were in accordance with the experimental results: the extension of the degraded region for wider devices occurs faster when the channel hot electron (CHE) injection mechanism (stress condition $V_{GS,stress} = V_{DS,stress}$) is dominant and slower in the stress regime $V_{th} \leq V_{GS,stress} \leq V_{DS,stress}/2$ (where the responsible device degradation mechanism is drain avalance hot carrier, DAHC). This is shown in Figures 4 and 5, respectively.

We suggest that the model predicts the maximum value of the threshold voltage of the two devices connected in series in the circuit equivalent, as it is expected for two devices connected in series. This implies that if the degradation is uniform, the corresponding threshold voltage will be equal for the two regions (defective and non defective), whereas if the damage is non-uniform (but more or less extended along the channel) the predicted threshold voltage of the whole device is, to a good approximation, that of the one at the defective channel region (which is the maximum one). This approximation is also supported theoretically in the relevant literature. According to Tang *et al* (Solid-State Electron. 2009; 53: 225-233), in a non-uniform channel (with a different local threshold voltage), the overall threshold voltage is the weighted threshold voltage over the channel (in our case the V_{th} of each device). However, as inversion in the defective channel part is harder to achieve, reflecting a much larger weight, the overall weighted threshold voltage is very close to the average threshold voltage of the defective channel part. Indeed, the threshold voltage as a parameter illustrates the mean concentration of free carriers and not how these carriers transport between source and drain. Moreover, the damage that occurs in the defective part of the channel region is reflected in two additional parameters: the defective region length ΔL, which is proportional to the interface state and / or the oxide trap states creation, and the mobility that charge carriers exhibit in the defective channel portion that depends on the defect charge density at the Si / SiO_2 interface and / or in the bulk oxide.

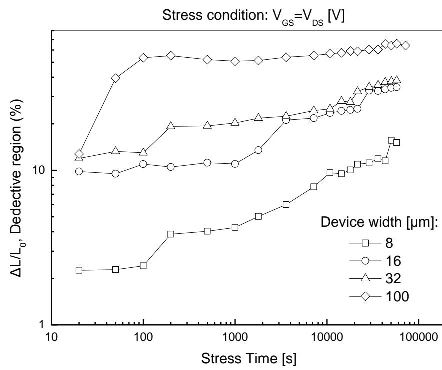


Fig. 4: Percentage variation of defective region length predicted from the model for devices of various widths W = 8, 16, 32 και 100 μm and of a common length (L = 0.8 μm). Stress condition: $V_{GS} = V_{DS}$.

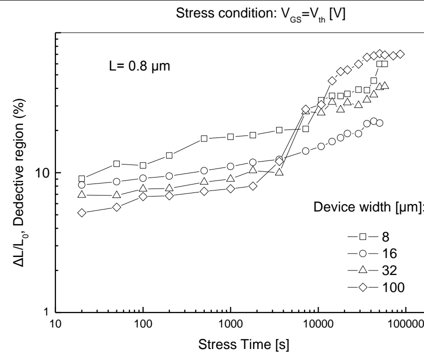


Fig. 5: Percentage variation of defective region length predicted from the model for devices of various widths W = 8, 16, 32 και 100 μm and of a common length (L = 0.8 μm). Stress condition: $V_{GS} = V_{th}$.

Figures 6 and 7 demonstrate the extracted threshold voltage shift (dot lines) and the overall threshold voltage shift predicted by the model (solid lines) for devices with different widths subjected to stress conditions $V_{GS,stress} = V_{DS,stress}$ and $V_{GS,stress} = V_{th}$, respectively. It is obvious (from both figures) that the model estimates the evolution of the threshold voltage of the stressed device adequately. It is noticeable that in Figure 6 the device with channel width of W = 100 μm exhibits the same behavior with the devices subjected to the stress condition $V_{GS,stress} = V_{DS,stress}$ (which is an initial decrease and then an increase of the threshold voltage; it is observed both in the extracted data and in the results of the model). Moreover, in order to gain insight of the degradation mechanisms existing in each case ($V_{GS,stress} = V_{DS,stress}$ and $V_{GS,stress} = V_{th}$), the threshold voltage parameter was also extracted by using the transconductance derivative method.

Considering the mobility that charge carriers have in each region, the quality of the Si/SiO_2 interface in the defective or the non-defective portion of the channel region affects its corresponding value. By applying the model, we evaluated the mean low field mobilities $\mu_{o,nd}$ and $\mu_{o,d}$ that the model takes into account for the two stressing conditions: $V_{GS,stress} = V_{DS,stress}$ and $V_{GS,stress} = V_{th}$.

In conclusion, the two main electrical stress conditions ($V_{GS,stress} = V_{DS,stress}$ and $V_{GS,stress} = V_{th}$) favor, respectively, the two main device degradation mechanisms due to hot carriers, that is, channel hot electron (CHE) and drain avalanche hot carrier (DAHC). A simple and practical electrical model predicting the device degradation under hot carrier stress was presented. The quality characteristics of the width depended degradation were evaluated by the model. More specifically, the defective region length was found to be width depended ΔL(W), with a different dependency for each stress regime. In the application of the model, out of the I_d-V_g characteristics taken for every aging step of the devices, we fit the model function, Equation (3), derived above. From the values we obtain ($V_{th,d}$, ΔL); then, we predict the values shown in Figures 6 and 7. Thus, the V_{th} shift (ΔV_{th}) of the overall device, approximately equal to the shift in $V_{th,d}$ (the maximum of the values $V_{th,d}$ and $V_{th,nd}$), is predicted by the model (this work is included in an IEEE TED paper currently in the publication process).

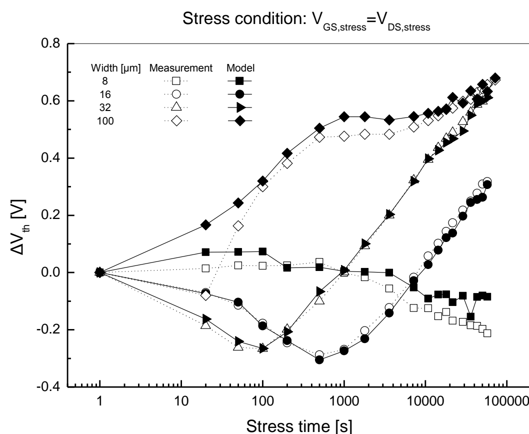


Fig. 6: Threshold voltage variation for devices of various widths W = 8, 16, 32 and 100 μm and of a common length (L = 0.8 μm). Stress condition: $V_{GS,stress} = V_{DS,stress}$. Extracted threshold voltage values (dot lines and open symbols) and predicted by the model (continues solid lines and filled symbols). Experimental (measured) data.

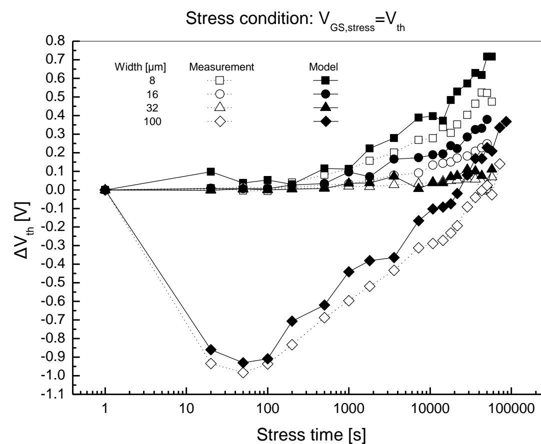


Fig. 7: Threshold voltage variation for devices of various widths W = 8, 16, 32 and 100 μm and of a common length (L = 0.8 μm). Stress condition: $V_{GS,stress} = V_{th}$. Extracted threshold voltage values (dot lines and open symbiols) and predicted by the model (continues solid lines and filled symbols).

C. Low temperature and transient current characterization

Based on the understanding of the transient currents in polycrystalline silicon TFTs gained through investigations that culminated during the past year, a new approach for experimental determination of band gap states density (DOS), by Deep Level Transient Spectroscopy (DLTS), has been presented. An asymmetric U-shaped distribution of states in the band gap has been obtained. The results are in agreement with theoretical predictions and others experimental observations.

The influence of the longitudinal grain boundaries on thin film transistor (TFT) characteristics have also been investigated as a function of temperature. Three types of behavior have been identified: i) parameters that are not affected by the number of boundaries in the channel (swing), ii) parameters that are crucially affected (mobility) and iii) parameters that their behavior is temperature dependent (leakage current). Therefore, it is concluded that the appropriate number of boundaries in the channel, hence the channel width, must be chosen according to the needs of the corresponding application.

Finally, the role of back gate on the front channel operation of p-channel double gate devices has been investigated. The results suggest that the presence of a back gate can significantly adjust the front gate parameters and also control their temperature dependence, allowing for a desirable electrical behavior of double gate TFTs in a wide temperature range.

D. Material / optical characterization

With the work conducted within the framework of this task, during 2009 we further investigated the polysilicon film itself, as this film results from each SLS ELA technique utilized, before any transistors are fabricated in it. We characterized several advanced SLS ELA films morphologically (SEM, AFM) and optically (UV-visible spectroscopy, spectroscopic ellipsometry, XRD analysis), in order to gather detailed information on their microstructure. The XRD data revealed that the different SLS ELA techniques give a material significantly differentiated, as far as its crystallinity is concerned, from both amorphous Si and crystalline Si, probably due to its special crystalline structure, which resembles that of allo-Si. This Si crystal modification is a structure similar to graphene and consists of lamellar crystals. Therefore, the special characteristics observed in these films could be attributed to the atom arrangement itself.

PROJECT OUTPUT IN 2009

Publications in International Journals

1. “On the study of p-channel thin-film transistors fabricated by SLS ELA crystallization techniques”, Exarchos, M.A., G.J. Papaioannou, D.C. Moschou, D.N. Kouvatsos, A. Arapoyanni and A.T. Voutsas, Thin Solid Films 517 (23), 6375, October 2009.
2. “Back gate influence on front channel operation of p-channel double gate polysilicon TFTs”, Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, Thin Solid Films **517** (23), 6364, October 2009.
3. “Degradation and lifetime estimation of n-MOS SLS ELA polycrystalline TFTs during hot carrier stressing – Effect of channel width in the region $V_{th} \leq V_{GS,stress} \leq V_{DS,stress}/2$”, Kontogiannopoulos, G.P., F.V. Farmakis, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, Semiconductor Science and Technology 24 (7), 0750271, July 2009.

Publications in Conference Proceedings

1. “The effect of small geometry on the degradation performance of SLS ELA polysilicon thin film transistors”, Kontogiannopoulos, G.P., M.A. Exarchos, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, Proceedings of the 29th International Display Research Conference IDRC ’09) / Eurodisplay 2009, Rome, Italy, September 2009.
2. “Short channel effects in SLS ELA polysilicon TFTs”, Proceedings of the 5th International Kontogiannopoulos, G.P., D.C. Moschou, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, Thin Film Transistors Conference (ITC ’09) / 2009 Society for Information Display Europe Chapter Meeting, Paris, France, March 2009.

International Conference Presentations

1. “On the optical and structural properties of advanced SLS ELA polycrystalline silicon thin films”, Moschou, D.C. N. Vourdas, D. Davazoglou, D.N. Kouvatsos, V.E. Vamvakas and A.T. Voutsas, European Materials Research Society Spring 2009 Meeting, Strasbourg, France, May 2009.

PhD Theses

1. “Development of thin film transistor fabrication technology optimized with respect to the polysilicon film structure resulting from the crystallization process”. Despina Moschou, Ph.D. degree awarded from the Department of Informatics, University of Athens
2. “Investigation of ageing degradation effects in polysilicon thin film transistors crystallized using advanced annealing techniques”, Giannis Kontogiannopoulos, Ph.D. degree awarded from the Department of Physics, University of Athens