Project II.2: MATERIALS AND DEVICES FOR MEMORY AND EMERGING ELECTRONICS

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Objectives

- Development of functional dielectrics and nanostructured materials for inorganic/organic memory and advanced electronic applications.
- Study of the structural and electrical properties of the generated materials and demonstration of material functionality enabling the development of emerging electronic devices.
- Realization and testing of electronic devices with emphasis on non-volatile memory cells.

Activities

Our research activities in materials and structures for memory applications started in 1996 with the development of the low-energy ion-beam-synthesis (LE-IBS) technique in collaboration with Salford University (UK). Two-dimensional arrays of Si nanocrystals in thin gate dielectrics were demonstrated and further exploited in the fabrication of nanocrystal memories (NCMs). This activity was first supported by the EU project, FASEM (1997-2000). LE-IBS development with target the realization of non-volatile NCMs in an industrial environment has been conducted further within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer, Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last few years to novel NCMs alternatives including: (a) Memory devices by Si^+ irradiation through poly-Si/SiO_2 gate stack, (b) Memory devices using Ge-NCs produced by MBE, (c) hybrid silicon-organic and SiGe-organic memories; this last activity was conducted within the framework of the EU project, FRACTURE (2001-2003), (d) Formation of Si NCs in thin SiO_2 layers by Plasma Immersion, (e) Wet oxidation of silicon nitride implanted with low-energy Si ions for ONO memory stacks, (f) MOS structures with low-energy Ge-implanted thin gate oxides, (g) Proton radiation tolerance of nanocrystal memories, (h) Fabrication and characterization of SiO_2 films with Si NCs obtained by stencil-masked LE-IBS, (i) Hybrid organic thin film transistor by laser-induced-forward-transfer, (j) Fluorene-based cross-bar organic memory devices, and (k) III-Nitrides quantum dots-resonant tunneling diodes as tunable wavelength UV-VIS phototodetectors .

The above activities were conducted in collaboration with CEMES/CNRS (FR), FZR Dresden and ZMD AG (DE), Aarhus University (DK), Durham University (UK), Ion-Beam-Services (IBS, FR), MDM-INFM (IT), LETI/CEA (FR), NTUA (GR), INSA Toulouse (FR), Cambridge NanoTech (USA), TEI Crete (GR), Ioannina University (GR), IMS/NCSR'D' (GR) and MRG/FORTH (GR).

In 2010, our main activities described hereafter were focused on the following tasks: (A) Space charge polarization in acid doped polymer matrices using time-domain dielectric spectroscopy, (B) High-k dielectrics stacks for advanced non-volatile memory devices, (C) III-Nitrides quantum dots for memory applications, (D) Fabrication and characterization of Ge diodes, (E) III-Nitrides resonant tunneling diodes

A. Space charge polarization in acid doped polymer matrices using time-domain dielectric spectroscopy

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Polymer electrolytes have received considerable attention for their applications in lithium-ion batteries, fuel cells, photoelectrochemical and electrochromic devices, and more recently in organic electronics. In the latter area, much effort has been directed towards electrolytic materials based gate dielectrics for the development of organic field-effect transistors operating at low voltage. Gate dielectrics which insure the double function of super-capacitor and non-volatile information storage element have recently been demonstrated using a stack made of a polymer layer doped with electrolytic molecules (ion conducting layer) and a polymer layer containing ion-trapping molecules (see Kapetanakis et al., Adv. Mater. 20, 4568, 2008, and Org. Elec. 10, 711, 2009). The memory functionality (especially in terms of programming characteristics) of devices employing such dielectrics strongly depends on the macroscopic transport properties of the ion conducting layer. This requires knowledge of the charge transport processes arising from the motion of the ions and their dependences on various parameters like temperature, humidity and film thickness. Such investigations can be conducted by means of impedance spectroscopy usually through frequency-domain measurements.

For low-frequency responding systems such as those under study (see below), it is interesting to examine the time-dependence current resulting from the application (polarization) or the removal (depolarization) of a step-function electric field. Little used in analysis of electrolytic materials, this technique allows monitoring in real time of space charge polarization phenomena and its potential advantage increases as the measurement range moves to long time domains (i.e. low frequency domains, typically below 1Hz).

This year, our efforts have been placed on the study of ion transport and polarization mechanisms in polymer blend electrolyte systems consisting of a polymethyl methacrylate (PMMA) matrix doped with polyoxometalate (POM, $H_3PW_{12}O_{40}$) molecules where the moving ions are in the form of protons. The electrical properties of this system were investigated by means of transient-current versus time response and capacitance-voltage (C-V) measurements using MIS capacitor structures. The polarization / depolarization phenomena and proton transport were examined as a function of temperature, humidity, POM concentration and film thickness.

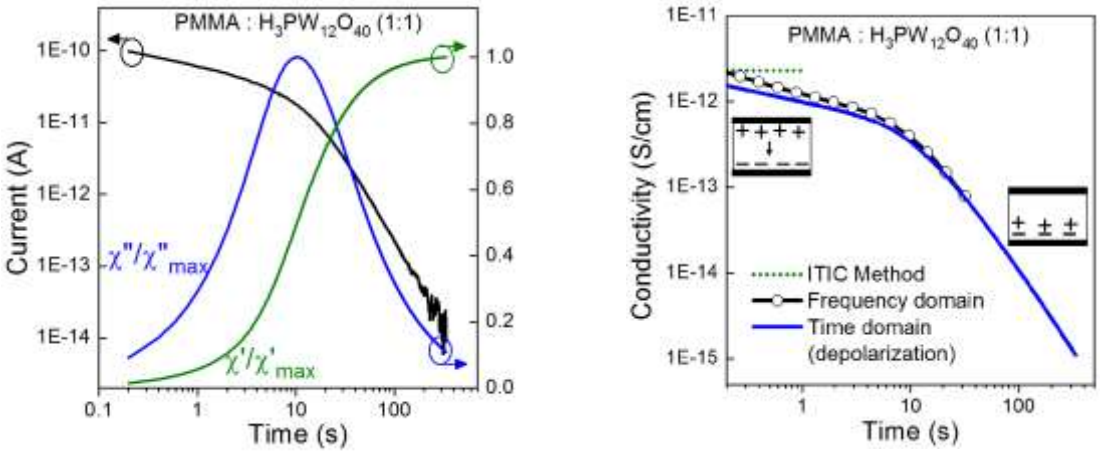

***Fig. 1**: (Left) Depolarization transient current response at 25ºC and imaginary (χ") / real (χ') parts of the time-dependent susceptibility obtained by Fourier transform. (Right) Conductivity vs time as extracted ($\sigma(\omega) = \varepsilon_0.\chi''(\omega).\omega$, $\omega=1/t$) from frequency- and time-domain measurements. The constant conductivity calculated using the Isothermal Transient Ion Current (ITIC) method is also shown for comparison purpose.*

B. High-k dielectrics stacks for advanced non-volatile memory devices

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The objective of this project is to examine the influence of advanced atomic layer deposition (ALD) precursor chemistry of high-k dielectrics, used as tunnel or blocking dielectrics of nitride-based memory structures. Replacement of one or more dielectric layers of the standard SONOS stack improves the functionality and performance of the resulting charge-trap memory device. This project is conducted in close collaboration with the University of Helsinki.

During the last year we conducted a systematic study of the structural and electrical properties of $SiO_2/Si_3N_4/ZrO_2$ or $SiO_2/Si_3N_4/HfO_2$ gate stacks with layer thicknesses of 2.5/5/10nm, respectively. Both high-k layers were deposited using two HfO_2 and ZrO_2 chemistries in combination with ozone as the oxygen source. Specifically for HfO_2: hafnium-tetrakis-ethylmethylamide (TEMAH) and bis methylcyclopentadienyl-methylmethoxy hafnium (HfD-04), and for ZrO_2: zirconium-tetrakis-ethylmethylamide (TEMAZ) and bis methylcyclopentadienyl-methylmethoxy zirconium (ZrD-04).

Electrical testing of MIS capacitors incorporating the above dielectric stacks showed that charge injection is controlled by the tunnel oxide thickness while the dielectric permittivity of the high-k layer determines the electric field distribution across the stack. These results indicate that the electrical properties extracted from J-V and C-V measurements as well as the charging characteristics and programming performance of the stacks can by grouped according to the high-k layer. While these properties exhibit small differences for the stacks under study, endurance measurements reveal that the alkylamides-processed samples can withstand significantly higher P/E cycles than those grown from the cyclopentadienyls (see Fig.2); thus indicating that the reliability of the high-k layers strongly depends upon the precursor choice.

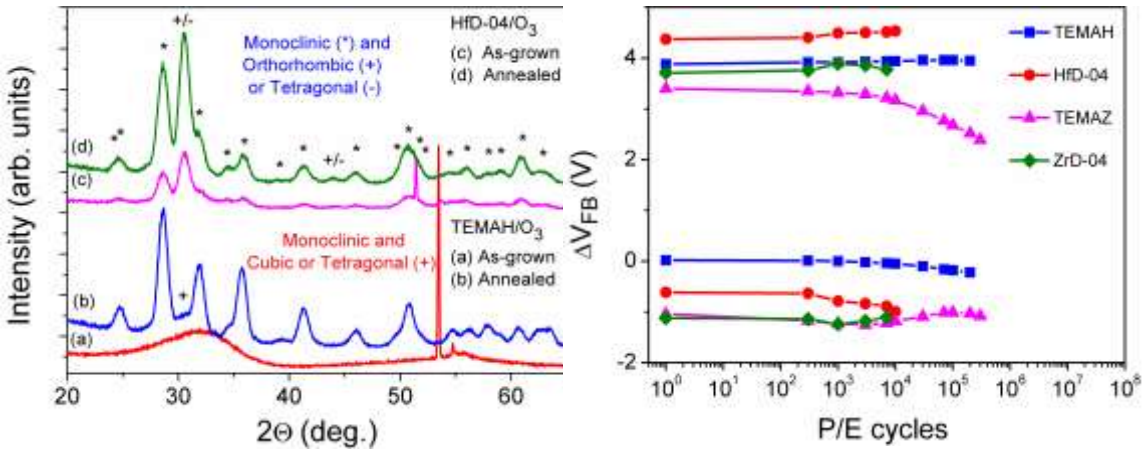

***Fig. 2**: (Left) Grazing Incidence X-Ray Diffraction patterns of $SiO_2/Si_3N_4/HfO_2$ gate stacks on a silicon substrate in the as-grown state and after annealing. (Right) Endurance characteristics of the HfO_2 and ZrO_2 based stacks in the 10V(P) and -11V(E) / 10ms regime.*

C. III-Nitrides quantum dots for memory applications

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The objective of these activities is to design, fabricate and evaluate a novel nanocrystal memory device based on III-Nitride materials. The device principle combines the advantages of charge storage into semiconductor quantum dots and their work function engineering. This can be achieved by forming semiconductor QDs exhibiting negative conduction band offset with respect to the substrate. In such case, the injected electrons can be trapped into the QDs at low voltage, while the retention time can be significantly improved due to the higher energy barrier the carriers have to overcome in order to tunnel back to the Si substrate. Assuming a Si substrate with a thin SiO_2 tunneling layer, gallium nitride (GaN) QDs fulfill these requirements.

In this direction, we focused our efforts on the realization of GaN-QDs structures on thin SiO_2 layers. The oxide layers - 3.5nm thick - were grown by dry oxidation of 100mm (100) n-Si substrates having a resistivity of 1-2 Ω·cm. The GaN-QDs were formed onto the SiO_2 films by radio frequency plasma assisted molecular beam deposition (RF-MBD). Two samples, A and B, with different QD sizes and density distributions were fabricated. The growth conditions have been varied properly in order to tune the size and the density of the QDs. PVD SiO_2 layers (~15nm thick) have been examined as capping dielectric. For the shake of comparison, a reference sample without QDs was fabricated.

The structural properties of samples A and B were conducted by means of TEM examination. A defocused XTEM image obtained from sample B is presented in Fig. 3l. Analysis of the above pictures allows for the extraction of the QD distribution characteristics. Sample A has a higher surface density compared to B, while the average size of QDs is ~5nm and ~3.5nm for samples A and B respectively.

Typical high frequency *C-V* characteristics measured on MOS capacitors from all fabricated samples are presented in Fig. 3r. Reference sample exhibits no hysteresis after a round voltage sweep. Contrary, the QD MOS capacitors exhibited strong hysteresis at relatively small voltages. Analysis of the related conductance characteristics in both samples A and B revealed that the investigated hysteresis is due to electron trapping into GaN-QDs.

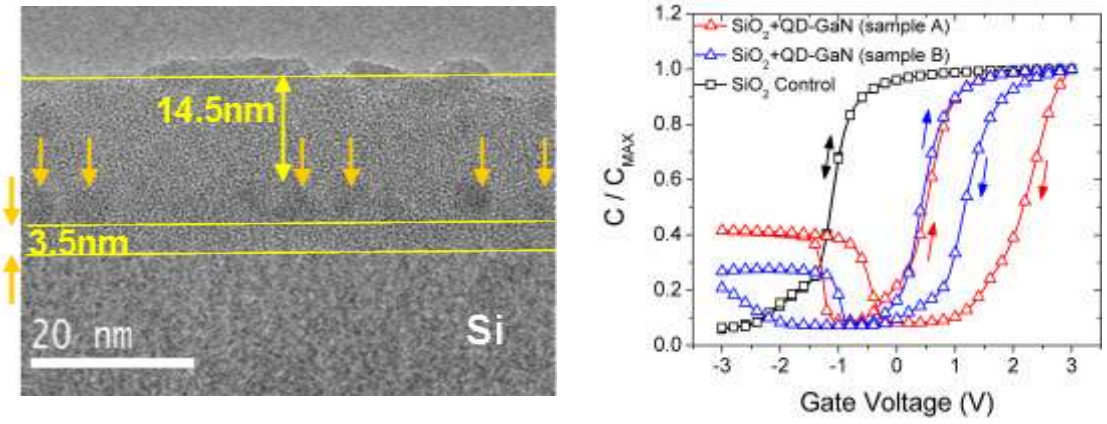

***Fig. 3**: (Left) Defocused XTEM image from the sample with 3.5nm SiO_2/GaN-QDs/ PVD SiO_2 stack on Si. (Right) Comparative normalized C-V (1MHz) plots from the control sample and the A and B samples with embedded GaN QDs at different densities.*

D. Fabrication and characterization of Ge diodes

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The objective of this research activity is the development of junction diodes on Ge substrates at temperatures lower than 400^{o}C. The severe scaling limitations of the conventional MOSFET fabricated on a Si substrate, and especially the limited drive current, require the replacement of the channel material. Germanium constitutes an attractive technological option due to the high mobility of both electrons (two times higher than Si) and holes (four times higher than Si). Although in terms of mobility, this material is ideally suited as channel material for high-performance logic applications, the germanium substrates integration technology faces significant challenges. A critical parameter is the formation of n+/p and p+/n junction diodes using low thermal budgets and low temperatures, a requirement to preserve the high-k dielectric integrity.

The diodes were formed by phosphorus or boron ion implantation using a dose of 2x10^{15} ions/cm^{2}. After implantation a 50nm-thick Pt layer was deposited on the diodes, followed by a thermal annealing either at 300 or 350^{o}C. SIMS measurements indicate that during annealing Ge diffuses into the Pt layer and Pt into the Ge layer, forming thus a platinum germanide layer which activates the dopants. Figure 4l shows the I-V characteristics of an n+/p diode after annealing at 350^{o}C for time intervals between 2 and 30 min. This year, our activities were focused on the study of the J-V and C-V characteristics as a function of temperature, of several p+/n and n+/p diodes processed using different annealing temperatures and times. In particular the reverse current and the depletion capacitance were analyzed to evaluate the main defect centers which may exist within the depletion region of the diodes. For this the reverse current and the depletion capacitance are separated into the bulk and peripheral components. Figure 4r shows the Arrhenius plot of the bulk current component of a p+/n diode annealed at 350^{o}C for 10 min. These characteristics of both n+/p and p+/n diodes reveal that the metal induced dopant activation process could resolve the issue of low temperature diode formation on germanium substrates.

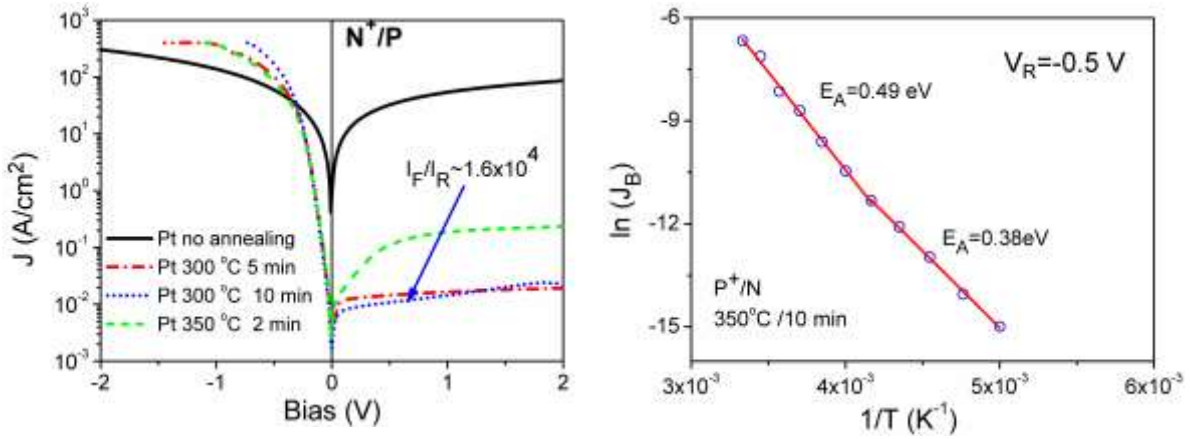

***Fig. 4**: (Left) J-V characteristics of p^{+}/n diode. (Right) Arrhenius plot of the reverse bulk current component (at V_R=-0.5V) of a p^{+}/n Ge diode.*

E. III-Nitrides resonant tunneling diodes

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These activities aim at the development of resonant tunneling diode (RTD) structures based on polar III-Nitrides heterostructures. Despite a number of research efforts, functional resonant tunneling diodes based on compound III-Nitride semiconductor heterostructures have not yet been demonstrated. Although negative differential resistance (NDR) characteristics have been reported, these effects disappear following the application of a single bias sweep through the NDR region that brings the devices in a lower conductivity state. The origin of this “charging” effect is not yet understood.

Clear evidence for the functionality of our RTD devices was presented two year ago (see 2008 IMEL annual report), while last year (2009 IMEL annual report) we reported on the effective reduction of the leakage current and the density of surface states that cause both NDR region screening and unexpected current switching to high values. This year, we focused our efforts on the optimization of the deposition conditions of the TEOS passivation layer as well as the electrical parameters that can be extracted from different characterization techniques.

In the I-V characteristics of fabricated symmetric (0001) Al(Ga)N/GaN DBRT diodes (Fig. 5l), two distinct behaviors were observed: (i) negative differential resistance associated with charging and (ii) strong multistability, depending on the composition of the barriers. In the case of heterostructures with high Al-content barriers, NDR-like IVs, with large peak-to-valley current ratios were obtained (Fig. 5r). However, as bias swept through the NDR region, the devices gradually charged and finally attained a metastable low-conduction status in which NDR transitions were completely washed out. In the case of lower Al-content barriers, an unstable behavior was observed, with abrupt transitions between different conductivity states. The former behavior is associated with the large asymmetry in the effective strength of collector and emitter side barriers and with the presence of 2DEG states. The latter one is in agreement with theoretical predictions of multistability in double barrier structures with quantized emitter region states. Further investigations are currently in progress to optimize the peak-to-valley ratio in the I-V characteristics of the latter devices.

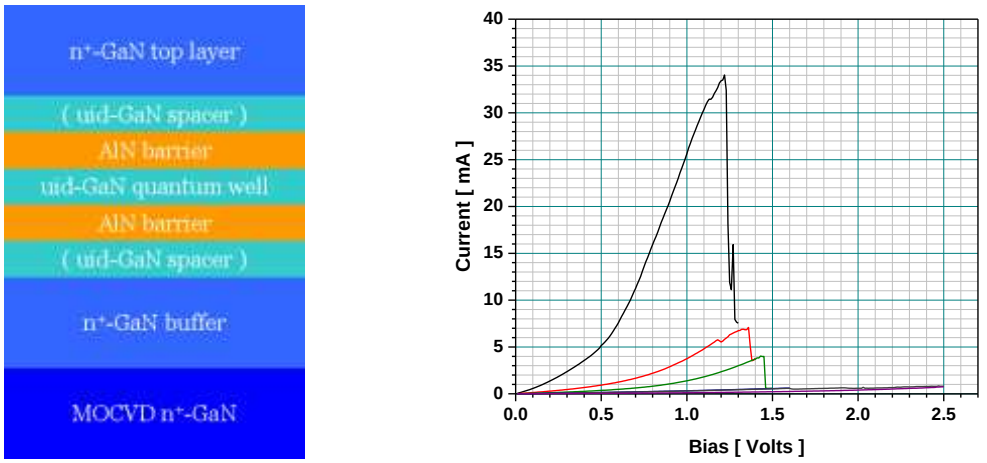

***Fig. 5**: (Left) Schematic of the investigated DBRTD structures. (Right) I-V curves exhibiting gradual charging in AlN/GaN DB resonant tunneling diodes.*

PROJECT OUTPUT IN 2010

Publications in International Conference Proceedings

1. “Charge trapping memories with atomic layer deposited high-k dielectrics capping layers”, N. Nikolaou, P. Dimitrakis, P. Normand, K. Giannakopoulos, K. Mergia, V. Ioannou-Sougleridis, K. Kukli, J. Niinistö, M. Ritala, M. Leskelä, Materials Research Society Symposium Proceedings 1250, 3-8 (2010).
2. “Annealing effects on Si nanocrystal nonvolatile memories”, P. Dimitrakis, C. Bonafos, S. Schamm-Chardon, G. BenAssayag, P. Normand, Materials Research Society Symposium Proceedings 1250, 23-28 (2010).
3. “Nanocrystal memory device utilizing GaN quantum dots by RF MBD”, P. Dimitrakis, E. Iliopoulos, P. Normand, Materials Research Society Symposium Proceedings 1250, 63-68 (2010).
4. “Formation of Ge nanocrystals in high-k dielectric layers for memory applications”, P. Dimitrakis, V. Ioannou-Sougleridis, P. Normand, C. Bonafos, S. Schamm-Chardon, A Mouti, B. Schmidt, J. Becker, Materials Research Society Symposium Proceedings 1250, 69-74 (2010).

Conference Presentations

1. “GaN quantum dots as charge storage elements for memory devices”, P. Dimitrakis, P. Normand, K. Tsagaraki, E.Iliopoulos, 19th European Workshop on Heterostructure Technology (HETECH 2010), 18-20 October, Fodele, Crete, Greece (2010).
2. “Implantation energy effect on photoluminescence spectroscopy of Si nanocrystals locally fabricated by stencil-masked ultra-low-energy ion-beam-synthesis in silica”, R. Diaz, C. Suarez, F. Gloux, C. Bonafos, S. Schamm, A. Arbouet, R. Marty, V. Paillard, J. Grisolia, P. Normand, P. Dimitrakis, G. BenAssayag, 17th International Conference on Ion Beam Modification of Materials (IBMM 2010), 22-27 August, Montreal, Canada (2010).
3. “Investigation of sulfonium salts as charge transport carriers for improvement of Polymer Light Emitting Diodes performance”, D. G. Georgiadou, P. Dimitrakis, M. Vasilopoulou, L. C. Palilis, L. Sygellou, S. Kennou, D. Dimotikali, P. Argitis, Micro&Nano 2010, 12-15 December, Athens, Greece (2010).
4. “Negative differential resistance and charge trapping phenomena in (0001) AlGaN/GaN double barrier resonant tunneling diodes”, G. Deligeorgis, P. Dimitrakis, Th. Kostopoulos, G. Konstantinidis, X. Dimizas, P. Normand, E. Iliopoulos, Micro&Nano 2010, 12-15 December, Athens, Greece (2010).
5. “Low temperature metal-induced dopant activation of Germanium N+/P and P+/N diodes”, V. Ioannou- Sougleridis, S.F. Galata, E. Golias, Th. Speliotis, A. Dimoulas, D. Giubertoni, S. Gennaro, M. Barozzi, E-MRS Spring Meeting 2010, June 7-11, Strasbourg, France (2010).
6. “Laser printing of polythiophene for organic electronics”, M. Makrygianni, P. Dimitrakis, P. Normand, S. Chatzandroulis, I. Zergioti, E-MRS 2010 Spring Meeting, June 7-11, Strasbourg, France (2010).

Edition of Conference Proceedings

1. C. Bonafos, Y. Fujisaki, P. Dimitrakis, E. Tokumitsu, «Materials and Physics of Nonvolatile Memories II», Mater. Res. Soc. Symp. Proc. Vol. 1250, Warrendale, PA, 2010.

Conference and Workshop Organization

1. C. Bonafos, Y. Fujisaki, P. Dimitrakis, E. Tokumitsu, “Materials and Physics of Nonvolatile Memories”, Symposium G, MRS Spring Meeting 2010, 5-9 April, San Francisco, CA, USA

Patent

1. European patent application, EP 2277202 (2010), in continuation of PCT/GR2009/000023 (2009), Memory devices using proton-conducting polymeric materials, Inventors: E. Kapetanakis, A.M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Normand.