Project III. 3: THIN FILM DEVICES for LARGE AREA ELECTRONICS

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Funding

- Sharp Labs of America grant, 2003 – 2005.
- Two GSRT bilateral Greece-Serbia projects, 2003 – 2007.
- PENED contract, project code 03ED550, 2005 – 2009.
- One postdoctoral fellowship (Dr. Moschou), 2010 – 2012.
- Currently, participation in IMEL cooperation project with Heliosphera (initiation in 2010). Two further proposals are under evaluation.

Objectives

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors (TFTs) fabricated in such films. Such advanced TFTs are necessary for next generation large area electronics systems, which are now in the research and development phase. Specifically, the targets of the project are:

- Evaluation of device parameter hot carrier and irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films with sequential lateral solidification (SLS).
- Investigation of the influence of the crystallization technique and the film thickness on TFT performance, defect densities and degradation for technology optimization.
- Investigation of effects of variations in TFT device structure and in the fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Assessment of material properties of ELA poly-Si TFTs using optical measurements.

MAIN RESULTS IN 2010

Task 1: Characterization of SLS ELA TFTs

Advanced polycrystalline silicon thin film transistors, such as devices fabricated at very low temperatures using sequential lateral solidification excimer laser annealing techniques, are essential for large area electronics and high performance flat panel displays. The objective of this task is the characterization of poly-Si TFTs having various technologically important structures and crystallized with different SLS ELA variations, as well as the determination of process parameters that affect device performance. We have studied the effect of the TFT active region film microstructure, relating the film characteristics themselves with the electrical performance and reliability characteristics of the TFTs. During 2010 we continued work on single gate SLS ELA TFTs that had been described in the previous two years and we elaborated, in new publications, on the use of the parameter $V_{g,max}$-V_{th} for the straightforward estimation of polysilicon active layer trap density. Moreover, we evaluated the TFT degradation model described last year and determined the dominant mechanisms for width dependent TFT degradation under various bias conditions (Kontogiannopoulos et al, IEEE Transactions on Electron Devices, ED-57 (6) 1390, June 2010). For both stress conditions ($V_{GS,stress} = V_{DS,stress}$ and $V_{GS,stress} = V_{th}$) the channel width was found to affect the intensity and not the mechanism of the device degradation; the degradation occurs faster: i) for wider devices at the condition $V_{GS,stress} = V_{DS,stress}$ (damage caused mainly by carrier trapping in the oxide through channel hot electron injection, CHE), ii) for narrower devices at the condition $V_{GS,stress} = V_{th}$ (damage caused mainly by drain avalanche hot carriers inducing interface state generation, DAHC). The defective region length ΔL was found to be width depended, with a different dependency for each stress regime. Table I qualitatively sums up the main results of the investigation of width dependent SLS ELA TFT degradation.

TABLE I

Stress Condition (Degradation Mechanism)	$V_{GS,stress} = V_{th}$ (DAHC)	$V_{GS,stress} = V_{DS,stress}$ (CHE)
Main reason of degradation mechanism enhancement	Drain-induced barrier lowering (DIBL)	Self-heating effects (SHE)
Enhancement of degradation as the channel width becomes	Narrower (W↓)	Wider (W↑)

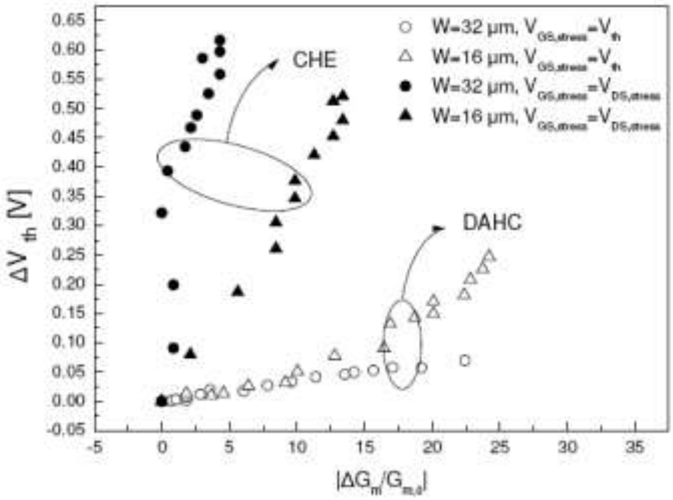


Fig. 1. Threshold voltage variation versus percentage variation of the maximum of transconductance for the tested geometries. Both stressing conditions are shown ($V_{GS,stress} = V_{DS,stress}$, $V_{GS,stress} = V_{th}$).

By plotting the extracted increase of ΔV_{th} versus the increase of $|\Delta G_{m,max}/G_{m,0}|$ (Fig. 1) for the devices with W = 16 μm and 32 μm stressed at $V_{GS,stress} = V_{th}$ or at $V_{GS,stress} = V_{DS,stress}$ (in the latter condition, this increase refers to the differences of threshold voltage and transconductance values compared to the values at the onset of CHE injection), it is noticed that there is a common degradation mechanism for all TFTs of different widths for each stress condition that depends only on the relative values of ΔV_{th} and $\Delta G_{m,max}$. As it is noticed, for the stress condition $V_{GS,stress} = V_{DS,stress}$, larger ΔV_{th} shifts are present for the same $|\Delta G_{m,max}/G_{m,0}|$ variations compared to the case of the stress condition $V_{GS,stress} = V_{th}$. Furthermore, for $V_{GS,stress} = V_{DS,stress}$ there is not a linear dependence (i.e. slope ≈ 1) between the threshold voltage variation and the transconductance degradation in the tested devices and as a result the uniform model of damage cannot be applied.

Task 2: Investigation of double gate TFTs

The presence of a second gate in advanced SLS ELA polysilicon TFTs offers additional possibilities, which cannot be realized with standard top or bottom gate devices, such as the control of TFT electrical parameters by appropriately biasing the bottom gate. During 2010, as the characterization of single gate TFTs made with the same technology was being completed, we continued the investigation of double gate TFTs with the aim of modeling their operation. These double gate devices currently being measured have varying lengths of both gates. Our scope is to determine the role of both gate lengths on TFT performance and electrical characteristics, probing possible short channel effects. For the purposes of the characterization and modeling of double gate TFTs, during 2010 we have secured a postdoctoral fellowship (Dr. Moschou), which began in February 2011. We have also initiated collaboration on DG TFTs with the University of Thessaloniki, where additional capabilities, such as cryogenic measurements, will be utilized.

Task 3: Material / optical characterization

The object of this work was to probe the optical properties of advanced SLS ELA poly-Si films. We employed three optical characterization techniques: UV-visible spectroscopy, spectroscopic ellipsometry and XRD analysis. Utilizing the Tauc-Lorentz model we obtained the film refractive index from UV-visible spectroscopy data and observed the much different behavior of the advanced SLS ELA films from a-Si ones. The significant difference of our films from also c-Si was probed through ellipsometry. Film XRD analysis showed a prevailing peak angle for all films at around 21.5^o, which, according to literature, corresponds to a Si modification named allo-Si. XRD spectra were acquired both from the front and from the back side of the samples, in order to ascertain that this prevailing peak is not an effect from the substrate. Indeed, front and back spectra (Fig. 2) show a difference with a prevailing peak at the aforementioned angle, thus verifying that this peak is not a substrate artifact. The above indicate that possibly SLS-ELA Si films have a crystallographic structure similar to allo-Si (grapheme-like), thus explaining the extremely high mobility values measured for TFTs fabricated in such films.

We continued our previous work studying SLS ELA polysilicon thin film microstructure, trying to further support this conclusion. We believe that the rapid melting and re-crystallization of the film could possibly cause mechanical stresses that modify the Si structure to this allo-Si form. Indeed, profilometry measurements showed that SLS ELA samples featured significant deflection. From this film deflection the applied stress was calculated through the relationship given by Glang et al (Rev. Sci. Instrum., 7 (1965) 36-1). Significant stress values were calculated for all of our SLS LA samples (Fig. 3), quantitatively supporting our assumption for mechanical stresses within the films. This could, also, be the reason for the broadness of the corresponding XRD peak.

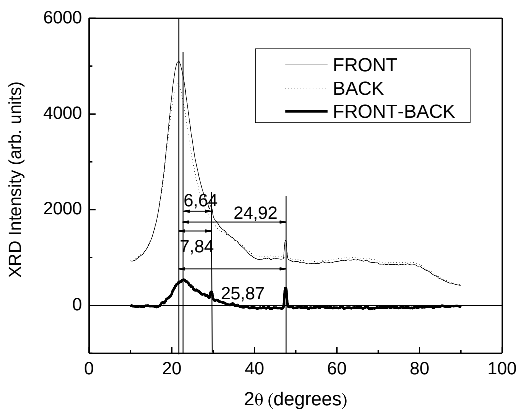
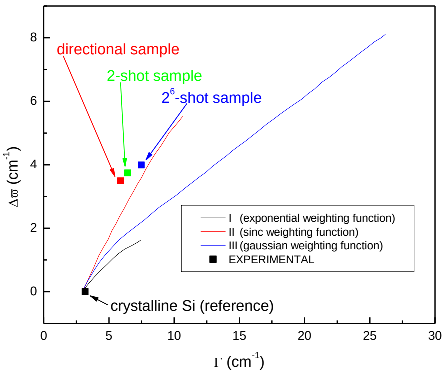


Fig. 2: XRD spectra for the three differently crystallized SLS ELA polysilicon films acquired both from the front and from the back side.

SAMPLE	**Stress σ (dynes/cm^2)**
Directional top	4.68×10^{10}
Directional bottom	7.65×10^{9}
2-shot top	7.29×10^{10}
2-shot bottom	1.21×10^{11}
2^6-shot top	6.69×10^{10}
2^6-shot bottom	1.07×10^{11}

Fig. 3: SLS ELA film stress σ calculated by profilometry.

In order to verify the presence of mechanical stresses within our samples we proceeded to their Raman analysis. We recorded their Raman spectra and extracted for each sample its Raman shift (Δω) and Raman linewidth (Γ). The plot of these Raman parameters and their comparison to documentation results can show whether there are mechanical stresses present in the studied films. Indeed, comparisons of our sample results to documentation results for several different weighting functions (Fig. 4) and different grain shapes (Fig. 5) revealed big differentiation for SLS ELA thin films, attributed again to mechanical stresses. We are currently studying further these results so as to clarify their exact meaning.



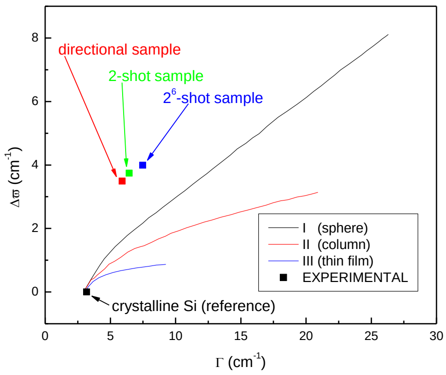


Fig. 4: Raman spectra results (Raman frequency shift Δω vs Raman linewidth Γ) for the three differently crystallized SLS ELA polysilicon films compared to equivalent documentation results for poly-Si films with three different weighting functions.

Fig. 5: Raman spectra results (Raman frequency shift Δω vs Raman linewidth Γ) for the three differently crystallized SLS ELA polysilicon films compared to equivalent documentation results for poly-Si films with three different grain shapes.

PROJECT OUTPUT IN 2010

Publications in International Journals

1. Moschou, D.C., Kontogiannopoulos, G.P., Kouvatsos, D.N., Voutsas, A.T., "On the importance of the $V_{g,max}$-V_{th} parameter on LTPS TFT stressing behavior", *Microelectronics Reliability* **50** (2), 190, February 2010.
2. Kontogiannopoulos, G.P., F.V. Farmakis, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, "A Practical Model Assessing the Degradation of Polycrystalline Silicon TFTs due to dc Electrical Stress", *IEEE Transactions on Electron Devices* **ED-57** (6), 1390, June 2010.
3. Despina Moschou, Nikolaos Vourdas, Dimitrios Davazoglou, Dimitrios Kouvatsos, Vassilis Emm. Vamvakas and Apostolos Voutsas, "On the optical properties of SLS ELA polycrystalline silicon films", *Microelectronic Engineering, in press*.
4. Despina Moschou, Filippos Farmakis, Dimitrios Kouvatsos and Apostolos Voutsas, "$V_{g,max}$ - V_{th}: A new electrical characterization parameter reflecting the polysilicon film quality of LTPS TFTs", *Microelectronic Engineering, in press*.
5. Michalas, L., M. Koutsoureli, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "Hydrogen passivation on sequential lateral solidified polysilicon TFTs", *Microelectronic Engineering, in press*.

International Conference Presentations

6. Despina Moschou, Filippos Farmakis, Dimitrios Kouvatsos, & Apostolos Voutsas, "*$V_{g,max}$ - V_{th}: A new electrical characterization parameter reflecting the polysilicon film quality of LTPS TFTs", 4th International Conference (Micro&Nano 2010) on Micro- Nanoelectronics, Nanotechnologies and MEMs*, NCSR Demokritos, Athens, 12-15 December 2010.
7. Despina Moschou, Nikolaos Vourdas, Dimitrios Davazoglou, Dimitrios Kouvatsos, Vassilis Emm. Vamvakas, & Apostolos Voutsas, "*On the optical properties of SLS ELA polycrystalline silicon films", 4th International Conference (Micro&Nano 2010) on Micro- Nanoelectronics, Nanotechnologies and MEMs*, NCSR Demokritos, Athens, 12-15 December 2010.
8. Michalas, L., M. Koutsoureli, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "Hydrogen passivation on sequential lateral solidified poly-Si TFTs", *4th International Conference on Micro- and Nanoelectronics, Nanotechnology and MEMS (MicroNano 2010)*, Athens, Greece, December 2010.