PROJECT II.1 NANOSTRUCTURES FOR NANOELECTRONICS, PHOTONICS AND SENSORS

Project leader: A. G. Nassiopoulou

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Phd students: P. Manoussiadis, P. Sarafis, I. Leontis, K. Valalaki

Others: E. Michelakaki (MSc), H. Katsogridakis (diploma thesis), M. Karmpadaki (administrative support)

Funding

- EU FP7 ENIAC JU Project SE2A, 1/1/2009-31/12/2011- Contract No 120009
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- EU FP7 Coordination and Support Action NANO-TEC, 1/9/2010-28/2/2013 - Contract No 257964

Research orientation

The activities of the group focus in the following:

a) Si nanowires, nanocrystals and their applications

The activity on semiconductor nanostructures started within this research group at the early nineties and is conducted within different EU projects. Worldwide pioneering results of the group in this field include the following: Light emitting Si nanopillars were first developed (APL 66(9), 1114 (1995), an electroluminescent device based on vertical Si nanowires was first developed (APL 69(15), 2267 (1996), the growth and investigation of the properties of single and multilayers of two-dimensional arrays of Si nanocrystals (NCs) with controllable size, embedded in SiO_2 was developed, Si NC memories with good characteristics using LPCVD Si nanocrystal synthesis was developed.

Currently, the group focuses on the following activities:

- Fabrication and properties of two-dimensional arrays of Si nanocrystals embedded in SiO_2 for solar cell applications
- SiNWs by metal-assisted chemical etching: synthesis, characterization and applications

b) Porous Si material technology and applications

The group has important expertise and know-how, as well as different proprietary processes in the field of porous Si material and technology. Existing processes include the fabrication of porous Si thick films formed locally on the Si substrate, porous Si free standing close-type membranes over cavity fabricated in a single electrochemical process and porous Si cantilevers and suspended membranes fabricated by electrochemistry. The porous material is composed of either randomly distributed pores or straight vertical pores. Pioneering results of the group in this field include the development of efficient porous Si micro-hotplate technology on the Si wafer, a low power Si flow sensor, a flow meter for the car engine and a system for respiration control using the low power flow sensor.

Currently the group develops applications of porous Si as a local substrate on the Si wafer for the on–chip integration of RF passive devices on the Si wafer.

c) Fabrication, properties and applications of porous anodic alumina thin films on Si

Porous anodic alumina thin films on Si with highly ordered hexagonally arranged pores are fabricated by electrochemistry and used either as template materials for growing nanowires and other nanostructures within the pores or as masking materials for Si nano-patterning. Porous anodic alumina is also used as a high-k dielectric material in memory devices and in metal-oxide-metal (MIM) capacitors.

Key results in 2011 within this activity are as follows:

- ⇨ The electrical transport and photocurrent in single and multilayered 2D arrays of Si nanocrystals for photovoltaic applications were investigated
- ⇨ The dielectric properties of porous Si microplates for use in on-chip local RF isolation were investigated in detail. Co-planar waveguides and inductors were fabricated on local porous Si areas on the Si wafer and tested at radiofrequencies
- ⇨ Charge trapping WORM memory devices using anodic alumina dielectric were fabricated and tested
- ⇨ A novel air flow meter for an automobile engine using a Si sensor with porous Si thermal isolation was fabricated and tested on a vehicle engine
- ⇨ The formation kinetics of Si nanowires by a single-step metal-assisted chemical etching process on lithographically defined areas on Si were investigated

Development of an electrochemistry laboratory and upgrading of the optical laboratory in 2011

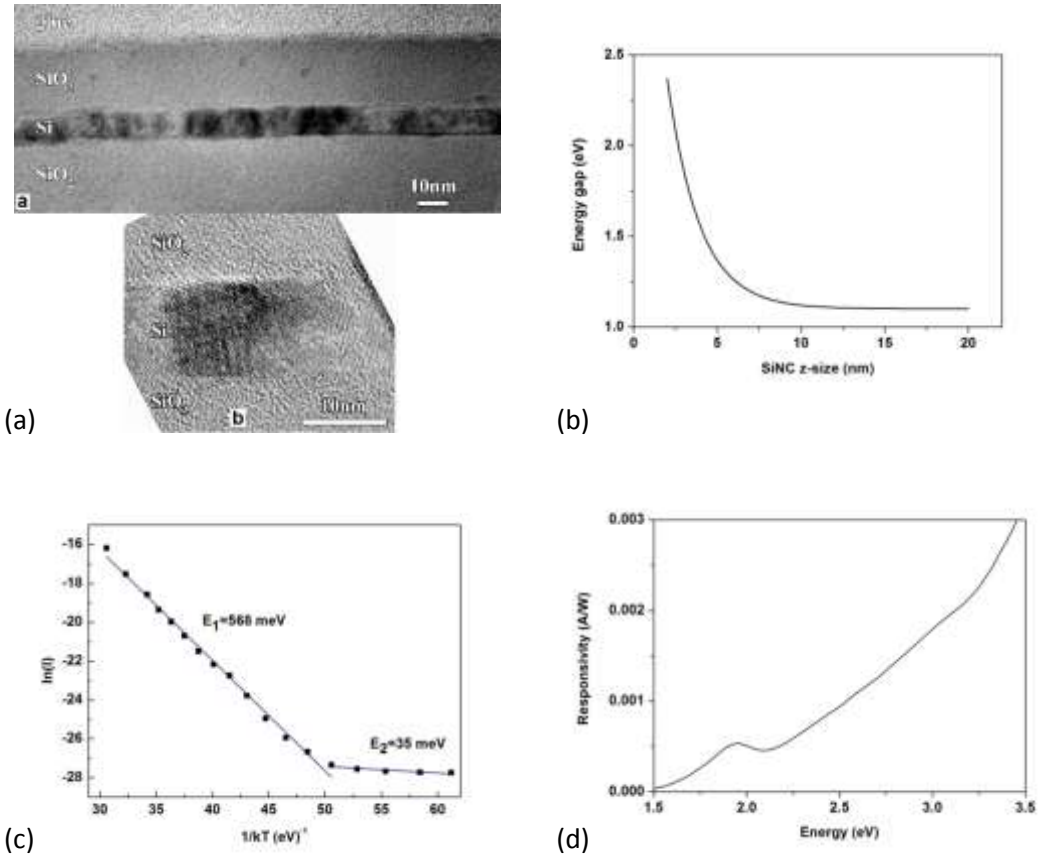
A new electrochemistry laboratory equipped with a chemical hook, different electrochemical cells and electronic control equipment was developed. The materials that are developed in the lab include porous Si, porous anodic alumina, Si nanowires by metal-assisted chemical etching, composites of porous Si with metal – filled vertical nanopores etc. A sputtering system is also available, dedicated to Cu and Pt thin films deposition.
The optical laboratory for PL, photocurrent and other solar cell measurements at room and low temperatures was also upgraded.

MAIN RESULTS IN 2011

A. Electrical transport and photocurrent in single and multilayered 2D arrays of Si nanocrystals for photovoltaic applications.

P. Manousiadis, S. Gardelis, and A.G. Nassiopoulou

We studied electrical transport and photocurrent in single and multilayers of two-dimensional silicon nanocrystal (SiNC) layers grown on quartz by low pressure chemical vapor deposition (LPCVD) and thermal oxidation steps. Our aim is to use such structures as absorber layers in silicon based photovoltaics of the 3rd generation. The SiNC layers consisted of SiNCs with columnar structure, i.e. with sizes in the z-direction equal to the layer thickness. The SiNCs within the layers were separated by grain boundaries. The structure and the dimensions of the SiNCs within the films were investigated by high resolution transmission electron microscopy and X-ray diffraction. From reflection and transmission measurements we were able to investigate absorption in the films. These results showed clearly an increase of the energy band gap with decreasing SiNC size, confirming that quantum size effects come into play as the SiNCs become smaller than the exciton Bohr radius in Bulk Si (~5 nm). Films containing very small SiNCs, smaller than the Bohr radius, which additionally were separated by silicon dioxide tunnel barriers, showed photoluminescence due to quantum confinement effects. Electrical transport showed that current is determined at low temperature by tunneling, whereas at higher temperatures by thermionic emission. Photocurrent showed similar dependence on photon energy with the absorbed light confirming that photocurrent is due to photo-generated carriers within the SiNCs when photon energy becomes higher than the energy band gap.



Figs. *(a) Transmission electron microscopy image of the films. (b) SiNC energy band gap as a function of z-size. (c) Temperature dependence of current. (d) Photocurrent as a function of photon energy.*

This work was published in JAP 109 (8), art. no. 083718 (2011)

B. Fabrication and characterization of a novel air flow meter for an automobile engine using a Si sensor with porous Si thermal isolation

A novel air flow meter for measuring the intake air of an automobile engine was demonstrated. It is based on a miniaturized silicon thermal mass flow sensor using a thick porous Si (Po-Si) layer for local thermal isolation from the Si substrate, on which the sensor active elements are integrated. The sensor shows high sensitivity and fast response and it is also robust, since it does not contain any free standing mechanical parts. Additionally, it is low cost since it uses Si processing batch technology in all its fabrication steps apart from porous Si formation. The sensor is mounted on one side of a printed circuit board (PCB), on the other side of which the readout and control electronics of the meter are mounted. The PCB with the sensor and electronics is fixed on a housing containing a semi-cylindrical flow tube, with the sensor situated in the middle of the flow tube. An important advantage of the present air flow meter is that it detects with equal sensitivity both forward and reverse flows. Two prototypes were fabricated, a laboratory prototype for flow calibration using mass flow controllers and a final demonstrator with the housing mounted in an automobile engine inlet tube. The final demonstrator was tested in real life conditions in the engine inlet tube of a truck. It shows an almost linear response in a large flow range between (6500 kg/h and +6500 kg/h), which is an order of magnitude larger than the one usually encountered in an automobile engine.

Fig. *(a): View of the interior of the automobile engine inlet tube with the air flow meter mounted in it.*

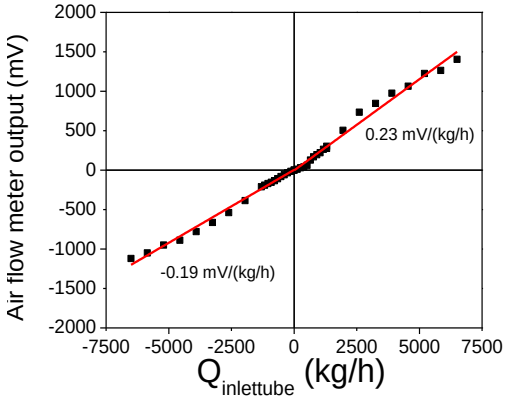


Fig. *(b): Calibration curve of the air flow meter output as a function of air flow through the engine air inlet tube. Black squares are the experimental data, while the red lines represent the linear fit to these data in the forward and reverse flow directions.*

C. Fabrication and characterization of charge trapping WORM memory structure using anodic alumina dielectric

A novel charge-trapping-type WORM memory structure using a 70 nm thick porous alumina layer on top of a p+ Si substrate (1-5 mΩcm) was demonstrated. During the fabrication process the formation of porous alumina by anodization is not stopped upon reaching the substrate but rather is continued so as to produce three different samples of three different SiO_2 layers at the interface between alumina and Si grown through the pores of the anodic alumina layer. We have shown that increasing the thickness of the electrochemical SiO_2 layer not only the memory window is increased but also the stability of operation of the device is improved. We have demonstrated that the WORM characteristics, in the case of the best sample, are a memory window of a factor of 100 in measured current, a good stability in terms of number of cycles, and retention of about a window of a factor of 45 after 10 years. We have also shown that the memories cannot be erased by the application of a negative pulse. We also noted that the devices have a yield of 100% and a spread of their characteristics of less than 10% for over 50 devices measured. The observed characteristics are attributed to the trapping of electrons at the SiO_2 layer. The fabrication process used for these devices is CMOS compatible and cost effective.

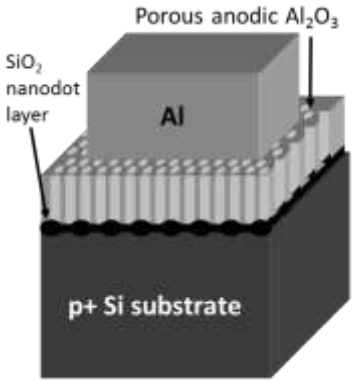


Fig. (a): *Schematic representation of a WORM device consisting of the p+ Si substrate, the porous Si/SiO_2 dielectric bilayer and the top Al contact.*

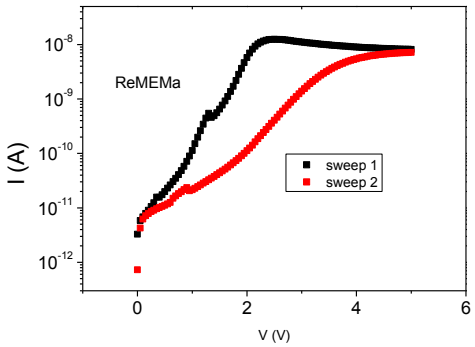


Fig. (b): *Current (I)-voltage (V) characteristics for the first and second voltage sweeps of sample ReMEM. The results are representative for all three samples.*

D. Porous Si microplate technology for on-chip local RF isolation

Using the process developed in 2010, co-planar wave guide (CPW) transmission lines were fabricated on porous Si microplates electrochemically developed on low RF loss substrates. The substrates used were p+ Si wafers of resistivity 0.001-0.005 Ωcm. The thickness of the porous Si microplate was 150 μm. The CPW lines were designed to have 2 different values of characteristic impedance, namely 50 and 145 Ω. The lines were characterized up to 40 GHz. De-embedding techniques were used to extract the values of the characteristic impedance, the quality factor and the attenuation constant. It was shown that attenuation lower than 0.3 dB/mm can be achieved at 40 GHz for both values of the characteristic impedance used. This value is several times better than commonly quoted values in the literature. Also a quality factor of 20 was demonstrated at 40 GHz. The experimental results were reproduced using simulations with the HFSS program. The CPW lines were then tested up to a frequency of 110 GHz, also producing state-of-the-art results in continuation of the work performed in 2010. The results were compared with the state-of-the-art results in the literature and a journal paper was written and published.

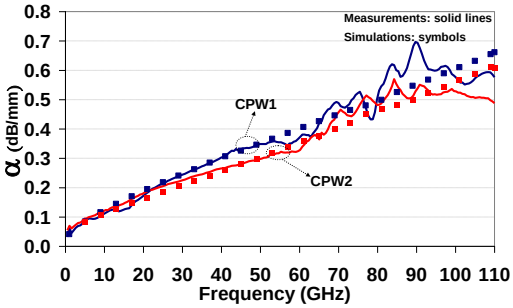


Fig. (a): *Measured attenuation loss of the two transmission lines investigated in this work versus frequency.*

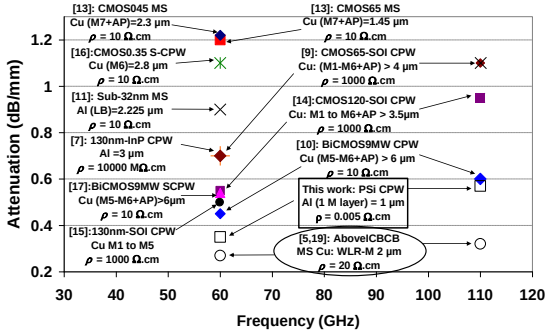


Fig. (b): *Published (state-of-the-art, see references in brackets) attenuation loss values of 50-Ω TLs realized using different technologies and topologies.*

Transactions on Electron Devices, Volume 58, Issue 11, pp. 3720-3724, Nov. 2011. Ref. "On-Chip High-Performance Millimeter-Wave Transmission Lines on Locally Grown Porous Silicon Areas," H. Issa, P. Ferrari, E Hourdakis, A. G. Nassiopoulou, IEEE

In addition porous Si thick films of different porosity were investigated by DC conductivity and RF measurements. In all cases the porous Si layers were produced by electrochemical dissolution of bulk p+ Si substrate with resistivity ~ 5 mΩcm. Moreover, CPWs were fabricated on them and characterized for frequencies up to 40 MHz. Using the measured S-parameters and simulations from the HFSS software program the values of the dielectric constant ε and the loss tangent tanδ were found. This particular project continues into 2012 in order to fine tune the extracted parameters of porous Si with different morphology and structure.

E. Si nanowires by a single-step metal-assisted chemical etching process on lithographically defined areas: formation kinetics

V. Gianneta and A. G. Nassiopoulou

The formation kinetics of Si nanowires [SiNWs] on lithographically defined areas using a single-step metal-assisted chemical etching process in an aqueous HF/AgNO3 solution were investigated within the group. It was shown that the etch rate of Si, and consequently, the SiNW length, is much higher on the lithographically defined areas compared with that on the non-patterned areas. A comparative study of the etch rate in the two cases under the same experimental conditions showed that this effect is much more pronounced at the beginning of the etching process. Moreover, it was found that in both cases, the nanowire formation rate is linear with temperature in the range from 20°C to 50°C, with almost the same activation energy, as obtained from an Arrhenius plot (0.37 eV in the case of non-patterned areas, while 0.38 eV in the case of lithographically patterned areas). The higher etch rate on lithographically defined areas is mainly attributed to Si surface modification during the photolithographic process.

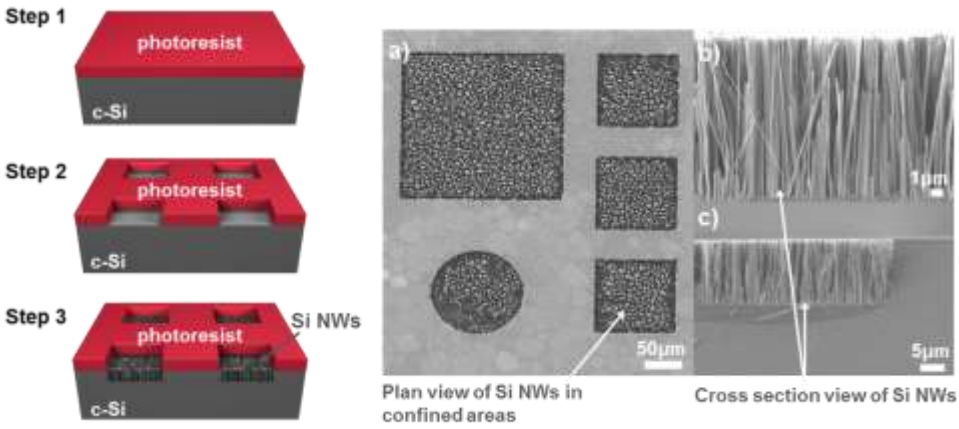


Fig.: *Schematic representation of processing steps (Step1-2: photolithography, Step3: Metal Assisted Chemical Etching and development of Si nanowires in confined areas). a)-c) SEM images of top view and cross section views of Si nanowires in confined areas.*

This work was published in Nanoscale Research Letters 2011, Vol **6**:597 with the title *"Si nanowires by a single-step metal-assisted chemical etching process on lithographically defined areas: formation kinetics"*.

Also part of it was presented in *XXVII Panhellenic Conference on Solid State Physics and Materials Science* which held in Limassol of Cyprus on 18-21 September 2011 as oral presentation.

Funding was received from the European Union's 7th Framework Programme (FP7/2007-2013) through the ICT NoE project 'Nanofunction' (grant agreement number 257375).

PROJECT OUTPUT IN 2011

Publications in International journals

1. "On-Chip High-Performance Millimeter-Wave Transmission Lines on Locally Grown Porous Silicon Areas", H. Issa, P. Ferrari, E. Hourdakis, A. G. Nassiopoulou, IEEE Transactions on Electron Devices 58 (11), pp. 3720-3724 (2011)
2. "High performance MIM capacitor using anodic alumina dielectric", E. Hourdakis and A. G. Nassiopoulou, Microelectronics Engineering, DOI: 10.1016/j.mee.2011.03.020 (2011)
3. "Charge trapping MOS memory structure using anodic alumina charging medium", E. Hourdakis and A. G. Nassiopoulou, Microelectronics Engineering 88 (7), pp. 1573-1575 (2011)
4. "Lateral electronic transport in 2D arrays of oxidized Si nanocrystals on quartz: Coulomb blockade effect and role of hydrogen passivation", P. Manousiadis, S. Gardelis and A. G. Nassiopoulou, Journal of Applied Physics 109 (8), art. no. 083718 (2011)
5. "Lateral electrical transport, optical properties and photocurrent measurements in two-dimensional arrays of silicon nanocrystals embedded in SiO_2", S. Gardelis, P. Manousiadis and A.G. Nassiopoulou, Nanoscale Research Letters 6 (1), pp. X1-6 (2011)
6. "Role of surface vibration modes in Si nanocrystals within light emitting porous Si at the strong confinement regime", M. Mahdouani, S. Gardelis, and A. G. Nassiopoulou, Journal of Applied Physics 110 (2), art. no. 023527 (2011)
7. "Silicon nanowires by a single-step metal-assisted chemical etching on lithographically defined areas: formation kinetics", A. G. Nassiopoulou, V. Gianneta and C. Katsogridakis, Nanoscale Research Letters, vol. 6 (1), 597 (2011)
8. "Electrical and structural properties of ultrathin SiON films on Si prepared by plasma nitridation", E. Hourdakis, A.G. Nassiopoulou, A. Parisini, M. A. Reading, J. A. Van Den Berg, L. Sygellou, S. Ladas, P. Petrik, A. Nutsch, M. Wolf and G. Roeder, Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures 29 (2), art. no. 022201 (2011)
9. "Optical characterization of nanocrystals in silicon rich oxide superlattices and porous silicon", E. Agocs, P. Petrik, S. Milita, L. Vanzetti, S. Gardelis, A. G. Nassiopoulou, R. Balboni and M. Fried, Thin Solid Films 519 (9), pp. 3002-3005 (2011)

10. "Nanomechanical properties of thick porous silicon layers grown on p- and p+-type bulk crystalline Si", C. A. Charitidis, A. Skarmoutsou, A. G. Nassiopoulou and A. Dragoneas, Materials Science and Engineering A 528 (29-30), pp. 8715-8722 (2011)

Edition of Conference Proceedings

1. "Proceeding of the PSST2010 Conference", held in Valencia in March 2011, Editors: A. Cantarero, M. Sailor, A. G. Nassiopoulou, P. Schmuki, L. Canham, Published in: Physica Status Solidi (C) Current Topics in Solid State Physics 8 (6), p.1723 (2011)
2. "Micro&Nano2010 - Special Symposium on Nanomaterials for sensing and energy harvesting devices", Edited by A. G. Nassiopoulou, Nanoscale Research Letters 6 (1), p. X1 (2011)
3. "Micro&Nano2010 - Proceedings of the International Conference on Microelectronics, Microsystems and Nanotechnology", Edited by A. G. Nassiopoulou, Microelectronic Engin., published online in 2011

Publications in International Conference Proceedings

1. "Electronic devices using porous anodic aluminum oxide", E. Hourdakis and A. G. Nassiopoulou, in: Physics, Chemistry and Applications of Nanostructures, Edited by V. E. Borisenko, S. V. Gaponenko, V. S. Gurin and C. H. Kam, published by World Scientific, containing the Proceeding of Nanomeeting 2011, p. 512, (2011)

Presentations in International Conferences – Invited talks

1. "Nanocrystalline systems and porous materials on Si for Electronics applications", **invited talk** presented by A. G. Nassiopoulou, XXVII Panhellenic Conference on Solid State Physics and Materials Science, Limassol, Cyprus, 18-21 September 2011
2. "Nanowires and nanostructured porous Si for novel applications in Electronics and photovoltaics", **Invited talk** presented by A. G. Nassiopoulou, 3rd International Conference IC4N, held in Crete island, Greece, 26-29 June 2011
3. "Low-dimensional materials for applications in Nanoelectronics, photovoltaics and sensors", **invited talk** presented by A. G. Nassiopoulou at the Workshop on the "Fabrication and characterization of nanomaterials and their applications", organized by the "Micro&Nano" Scientific Society, Thessaloniki, 3 March 2011
4. "High performance passive RF devices on a local porous Si substrate on the Si wafer", **invited talk** presented by A. G. Nassipoulou at the Workshop on "Current trends in Nanoelectronics" organized by the "Micro&Nano" Scientific Society and the Nano-dema Network, Patras, 25 February 2011
5. "Nanowires, nanodots and nanoporous materials for applications in Nanoelectronics and Sensors", **Invited colloquium** presented by A. G. Nassiopoulou at the Univ. of Ioannina on the 5th of April 2011
6. "Transport, optical and photo-electric properties of 2D arrays of Si nanocrystals embedded in SiO_2 for solar cell applications", S. Gardelis, P. Manousiadis and A. G. Nassiopoulou, Villa Conference on Energy and Enviromental Research, 21-25 April 2011, Las Vegas, Nevada, US, **invited talk** presented by Spiros Gardelis
7. "Electro-Optical properties of two-dimensional arrays of Si nanocrystals for solar cell applications", S. Gardelis, P. Manousiadis and A. G. Nassiopoulou, 8th International Conference on Nanosciences and Nanotechnologies, 21-15 July 2011, Thessaloniki, Greece, **invited talk** presented by Spiros Gardelis
8. "Silicon nanostructures for optoelectronic and photovoltaic applications", S. Gardelis, P. Manousiadis and A. G. Nassiopoulou, Nanotechnology and Materials Science and Engineering Multinational Workshop, 27-28 June 2011, University of North Texas, Denton, Texas, USA, **invited talk** presented by S. Gardelis
9. "Electrical and Optical Properties of 2D arrays of Silicon Nanocrystals", P. Manousiadis, S. Gardelis and A. G. Nassiopoulou, XXVII Panhellenic Conference on Solid State Physics and Materials Science, 18-21 September Limassol 2011, Cyprus, oral presentation by Pavlos Manousiadis
10. "Electronic devices using porous anodic aluminum oxide" Hourdakis E. and Nassiopoulou A.G., **Invited talk** presented by M. Hourdakis at the International Conference Nanomeeting 2011, Minsk, Belarus
11. "Si Nanowires in a single-step metal-assisted chemical etching. Properties and characterization", V. Gianneta and A. G. Nassiopoulou, (oral presentation by Violetta Gianneta), XXVII Panhellenic Conference on Solid State Physics and Materials Science, Limassol, Cyprus, 18-21 September 2011

MSc Thesis

1. I. Leontis, "PL-induced oscillations from porous anodic alumina on Si", supervised by A. G. Nassiopoulou, defended at the University of Thessaloniki, March 2011

Diploma Thesis

1. Charalambos Katsogridakis, "Growth of Si nanowires by metal-assisted chemical etching", Supervised by A. G. Nassiopoulou, defended at the University of Ioannina, April 2011

Courses taught

1. Lectures on "Silicon processing for Nanoelectronics" by A. G. Nassiopoulou within: a) the MSc program on Microelectronics organized by the Department of Informatics of the University of Athens, in cooperation with the Institute of Microelectronics of NCSR Demokritos and b) the MSc program on "Microsystems and Nanoelectronics" organized by the National Technical University of Athens with the participation of the Institute of Microelectronics of NCSR Demokritos
2. Lectures on "Micromechanics and Sensors", by the S. Gardelis within the MSc program organized by the Department of Informatics, University of Athens, in cooperation with the Institute of Microelectronics of NCSR "Demokritos"