Project II.2: MATERIALS AND DEVICES FOR MEMORY AND EMERGING ELECTRONICS

Project leader: P. Normand
Key researchers: V. Ioannou-Sougleridis, P. Dimitrakis
Collaborating Researchers: P. Argitis, N. Glezos, A.M. Douvas
PhD candidates: P. Goupidenis, N. Nikolaou
Graduate Students: D. Simatos, V. Poulakis

Objectives
- Development of functional dielectrics and nanostructured materials for inorganic/organic memory and advanced electronic applications.
- Study of the structural and electrical properties of the generated materials and demonstration of material functionality enabling the development of emerging electronic devices.
- Realization and testing of electronic devices with emphasis on non-volatile memory cells.

Activities
Our research activities in materials and structures for memory applications started in 1996 with the development of the low-energy ion-beam-synthesis (LE-IBS) technique in collaboration with Salford University (UK). Two-dimensional arrays of Si nanocrystals in thin gate dielectrics were demonstrated and further exploited in the fabrication of nanocrystal memories (NCMs). This activity was first supported by the EU project, FASEM (1997-2000). LE-IBS development with target the realization of non-volatile NCMs in an industrial environment has been conducted further within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer, Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last few years to novel NCMs alternatives including: (a) Memory devices by Si+ irradiation through poly-Si/SiO2 gate stack, (b) Memory devices using Ge-NCs produced by MBE, (c) hybrid silicon-organic and SiGe-organic memories; this last activity was conducted within the framework of the EU project, FRACTURE (2001-2003), (d) Formation of Si NCs in thin SiO2 layers by Plasma Immersion, (e) Wet oxidation of silicon nitride implanted with low-energy Si ions for ONO memory stacks, (f) MOS structures with low-energy Ge-implanted thin gate oxides, (g) Proton radiation tolerance of nanocrystal memories, (h) Fabrication and characterization of SiO2 films with Si NCs obtained by stencil-masked LE-IBS, (i) Hybrid organic thin film transistor by laser-induced-forward-transfer, (j) Fluorene-based cross-bar organic memory devices, and (k) III-Nitrides quantum dots-resonant tunneling diodes as tunable wavelength UV-VIS photodetectors.

The above activities were conducted in collaboration with CEMES/CNRS (FR), FZR Dresden and ZMD AG (DE), STMicroelectronics (IT), Aarhus University (DK), Durham University (UK), Ion-Beam-Services (IBS, FR), MDM-INFM (IT), LETI/CEA (FR), NTUA (GR), INSA Toulouse (FR), Cambridge NanoTech (USA), TEI Crete (GR), Ioannina University (GR), IMS/NCSR “D” (GR), University of Helsinki (FI) and MRG/FORTH (GR).

In 2011, our main activities described hereafter were focused on the following tasks: (A) Space charge polarization in acid doped polymer matrices using time-domain dielectric spectroscopy, (B) High-k dielectrics stacks for advanced non-volatile memory devices, (C) GaN quantum dots nanofloating gate memory devices, (D) Fabrication and characterization of Ge diodes, (E) Formation of Si nanocrystals in thin SiO2 layers by plasma-immersion ion-implantation.
MAIN RESULTS IN 2011

A. Space charge polarization in acid doped polymer matrices using time-domain dielectric spectroscopy

P. Goupidenis, P. Normand, A.M. Douvas, P. Dimitrakis, P. Argitis, E. Kapetanakis¹, V. Saltas¹, K. Beltsios², C. Pandis³, A. Kyritsis³, P. Pissis³

¹Department of Electronics, Technological Educational Institute of Crete
²Department of Materials Science Engineering, University of Ioannina
³Department of Physics, National Technical University of Athens

We recently demonstrated gate dielectrics which insure the double function of super-capacitor and non-volatile information storage element using a stack made of a polymer layer doped with electrolytic molecules (ion conducting layer) and a polymer layer containing ion-trapping molecules (see Kapetanakis et al., Adv. Mater. 2008, and Org. Elec. 2009). The memory functionality of such devices depends on the macroscopic transport properties of the ion conducting layer. This requires knowledge of the charge transport processes arising from the motion of the ions and their dependences on various parameters like temperature and humidity. For low-frequency responding systems such as those under study (see below), it is interesting to examine the time-dependence current resulting from the application (polarization) or the removal (depolarization) of a step-function electric field. This technique allows monitoring in real time of space charge polarization phenomena and its potential advantage increases as the measurement range moves to long time domains.

Last year, our efforts have been placed on the study of ion transport and polarization mechanisms in polymer blend electrolyte systems consisting of a poly(methyl methacrylate) (PMMA) matrix doped with polyoxometalate (POM, H₃PW₁₂O₄₀) molecules where the moving ions are in the form of protons. The properties of this system were investigated by means of transient-current versus time response and capacitance-voltage measurements using MIS capacitor structures. Interesting results have been obtained but it was difficult to draw definitive conclusions on the observed phenomena due to the non-metal behavior of the Si substrate. This year, we developed MIM-type capacitors specially designed for DC current minimization. Despite the difficulty in controlling the water content of the polymeric system, excellent results were obtained from measurements in the time and frequency response domains (Fig.1) performed in two laboratories. Both the MIM devices and the measurement set-up we developed, which allows current detection in the 10fA range, are well-suited to safely examine the polarization/depolarization phenomena and proton transport as a function of temperature, humidity, POM concentration and film thickness.

Fig. 1. (Left) Polarization and depolarization transient current responses at 23ºC; Inset: imaginary (χ") and real (χ') parts of the susceptibility as measured in the frequency response domain (FRD) and extracted from the time response domain (TRD, FFT of the I-V curve). (Right) Depolarization current responses (l) for different applied polarization voltages (V) after 30min/120ºC annealing. Inset: I / V vs time curves showing that the response function is independent on the applied electric-field strength.
B. High-k dielectrics stacks for advanced non-volatile memory devices


1Institute of Materials Science, IMS-NCSR ‘Demokritos’
2Institute of Nuclear Technology and Radiation Protection, IRTRP-NCSR ‘Demokritos’
3Chemical Department of Helsinki University (FI)

The objective of this project is to examine the influence of advanced atomic layer deposition (ALD) precursor chemistry of high-k dielectrics, used as tunnel or blocking dielectrics of nitride-based memory structures. Replacement of one or more dielectric layers of the standard oxide-nitride-oxide (ONO) stack of SONOS memory leads to charge trapping devices with improved memory functionality and performance. This project is conducted in close collaboration with the University of Helsinki.

This year our main activity focused on:

a) Testing of SiO$_2$/Si$_3$N$_4$/ZrO$_2$ or SiO$_2$/Si$_3$N$_4$/HfO$_2$ gate stacks with layer thicknesses of 2.5/5/10nm, respectively. Both high-k layers were deposited using two HfO$_2$ (TEMAH, HfD-04) and ZrO$_2$ (TEMAZ, ZrD-04) chemistries in combination with ozone as the oxygen source. Emphasis was placed on the endurance to write/erase cycling and charge retention (see Fig. 2) of test capacitors incorporating the above dielectric stacks. These studies complete our structural and electrical investigations in this area which started in 2009.

b) Study of SiO$_2$/Si$_3$N$_4$/Al$_2$O$_3$ (3.5/7/15nm in thickness) gate stacks, where the ALD Al$_2$O$_3$ layer was deposited using TMA (trimethylaluminium) and two different oxygen sources (ozone and water). Our investigations concentrated on the structural (TEM) and electrical properties (I-V, C-V) of these new dielectric stacks. Electrical examination was carried out using metal (Pt) gate capacitors. First results suggest that the TMA/O$_3$ process provides Al$_2$O$_3$ films materials with better insulating properties than the TMA/H$_2$O and is less sensitive to the over-erase affect.

![Fig. 2.](image)

**(a)** Charge retention characteristics of SiO$_2$/Si$_3$N$_4$/HfO$_2$ gate stacks. (b) Write and erase states of SiO$_2$/Si$_3$N$_4$/Al$_2$O$_3$ gate stacks.
C. GaN quantum dots nanofloating gate memory devices

P. Dimitrakis, P. Normand, E. Papadomanolaki\textsuperscript{1}, E. Iliopoulos\textsuperscript{1,2}, C. Bonafos\textsuperscript{3}

\textsuperscript{1} Department of Physics, University of Crete (GR)
\textsuperscript{2} MRG-FORTH (GR)
\textsuperscript{3} CEMES-CNRS, Université de Toulouse (FR)

The objective of these activities is to design, fabricate and evaluate a novel nanocrystal memory device based on III-Nitride materials. These devices exploit the charge storage capacity of semiconductor quantum dots (QDs) which exhibit negative conduction band offset with respect to the substrate. In such case, the injected electrons can be trapped into the QDs at low voltage, while the retention time can be significantly improved due to the higher energy barrier the carriers have to overcome in order to tunnel back to the Si substrate. Assuming a Si substrate with a thin SiO\textsubscript{2} tunneling layer, gallium nitride (GaN) QDs fulfill these requirements.

In this direction, we focused our efforts on the realization of GaN-QDs structures on thin SiO\textsubscript{2} layers. The oxide layers - 3.5nm thick - were grown by dry oxidation of 100mm (100) n-Si substrates having a resistivity of 1-2 Ω cm. The GaN-QDs were formed onto the SiO\textsubscript{2} films by radio frequency plasma assisted molecular beam deposition (RF-MBD). Samples with different Ga and N doses were fabricated in order to investigate the evolution of the QD size and density distribution. Following, a SiO\textsubscript{2} layer (~20nm thick) was deposited (LPCVD) to cap the Ga-N dots. For the sake of comparison, a reference sample without QDs and exposed to N beam flux was fabricated. MESA isolated Al gate MOS memory capacitors were fabricated for electrical characterization.

The structural properties of the samples with the lowest (see Fig. 3L) and the highest deposited Ga/N doses (not shown here) were investigated by cross-sectional transmission-electron-microscopy (TEM). These analyses revealed that in the first case the mean QD size and surface density were 3.5nm and 10\textsuperscript{12} cm\textsuperscript{-2}, respectively, while a continuous poly-crystalline GaN layer forms in the case of the highest dose sample.

High frequency (1MHz) C-V characteristics measured on MOS capacitors from all fabricated samples exhibited strong electron trapping efficiency leading to large memory windows. Nevertheless, negligible hole trapping was detected. No hysteresis effect was detected for the reference sample. The largest memory window was obtained from sample with the lowest dose. In that case, charge retention measurements at room temperature (Fig.3R) clearly indicated that the stored electrons can be retained for more than ten years. The charge loss rate is about 0.25V/dec suggesting that GaN-QDs are attractive for nano-floating gate memories.

![Cross-sectional TEM image and room temperature charge retention measurements](image)

**Fig. 3.** (Left) Cross-sectional TEM image and (Right) room temperature charge retention measurements after a programming pulse +15V/100ms. Insets denote the MESA isolated tested memory capacitors and a high resolution TEM image of the GaN-QDs. All results were obtained from sample with the lowest deposited Ga/N dose.
D. Fabrication and characterization of Ge diodes

N. Poulakis, V. Ioannou-Sougleridis, P. Normand, P. Dimitrakis, A. Dimoulas\(^1\), D. Giubertoni\(^2\), S. Gennaro\(^3\), M. Barozzi\(^2\), E. Simoen\(^3\)

\(^{1}\)Institute of Materials Science NCSR ‘Demokritos’
\(^{2}\)CMM-Irst, Fondazione Bruno Kessler, Trento, Italy
\(^{3}\)IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

The objective of this research activity is the development of junction diodes on Ge substrates at temperatures lower than 400\(^0\)C. High mobility substrates are considered as a solution to the severe limitations (especially in terms of drive current) in MOSFET performance scaling. However, Ge front end technology faces two main problems: The surface passivation of n-channel MOSFET and the formation of n+/p junction diodes at low thermal budgets due to the fast diffusion of n-type dopants. Our approach for fabricating such n+/p Ge diodes is based on platinum-assisted-dopant activation (V. Ioannou-Sougleridis et al. Essderc 2009). According to this original approach, a Pt layer (typically 50nm-thick) is first deposited on top of phosphorus or boron-implanted selected Ge regions. Then, the structures are annealed at low temperatures typically within 300-350\(^0\)C. The end result is the formation of a junction diode with high forward drive current and acceptable levels of reverse leakage currents.

This year, we concentrated our efforts on: (a) The separation of the current and capacitance components of the reverse current and capacitance characteristics in order to determine the bulk current as a function of the depletion width (see Fig. 4), from which it is possible to calculate the diffusion current, the generation lifetime and the recombination lifetime. (b) The temperature dependence of these parameters as a function of temperature. (c) The examination of the trap characteristics of the n+/p and p+/n diodes using deep-level transient spectroscopy.

![Image](image.png)

**Fig. 4.** Plot of bulk current density as a function of the depletion width of \(\text{p}^+ \text{n}\) diode for a set of 5 samples (a). Arrhenius plot of the diffusion current for a \(\text{p}^+ \text{n}\) Ge diode annealed at 350\(^0\)C for 10 min.
E. Formation of Si nanocrystals in thin SiO\textsubscript{2} layers by plasma-immersion ion-implantation

P. Normand, P. Dimitrakis, V. Ioannou-Sougleridis, E. Kapetanakis\textsuperscript{1}, F. Torregrosa\textsuperscript{2}, Y. Spiegel\textsuperscript{3}, C. Bonafos\textsuperscript{3}, G. Ben Assayag\textsuperscript{4}, A. Slaoui\textsuperscript{4}

\textsuperscript{1}Department of Electronics, Technological Educational Institute of Crete (GR)
\textsuperscript{2}Ion-Beam-Services, Peynier (FR)
\textsuperscript{3}CEMES-CNRS, Toulouse (FR)
\textsuperscript{4}InESS-CNRS, Strasbourg (FR)

Six years ago, we initiated research activities aiming at the development of a new Si-nanocrystal (Si-NC) synthesis route based on the plasma-immersion ion-implantation (PIII) technique. These activities were conducted in collaboration with CEMES/CNRS and one French SME (Ion Beam Services, IBS) in the framework of a bilateral French-Greek Project (ΕΡΑΝ.Μ.4.3.6.1Ε). While more research work was needed to provide reliable fabrication processes, the basic conditions required for the PIII-assisted synthesis of Si-NCs in SiO\textsubscript{2} thin films were established. The last three years, the R&D PIII activities conducted at IBS and CNRS, which associated the development of the IBS-PIII tool, PULSION®, and the use of specific precursors and plasma conditions, have recently conducted to the realization of Si-NCs 2D-arrays in SiO\textsubscript{2} matrices. This year a new framework between IBS, three CNRS Institutes (CEMES, CIMAP, InESS) and IMEL/NCSR/D has been established (Confidentiality Agreement June 30th 2011) to evaluate and optimize the PIII-produced-Si-NCs materials for the purpose of their exploitation in Flash-type memory devices or other emerging areas like NC solar cells. Our team is in charge of the production of Si wafers with ultra-thin thermally grown SiO\textsubscript{2} layers, is involved in the post-PIII processing steps and is responsible for the fabrication, electrical characterization and memory testing of the produced Si-NC dielectrics.

PROJECT OUTPUT IN 2011

Publications in International Journals


Publications in International Conference Proceedings


Conference Presentations


Edition of Conference Proceedings


Conference and Workshop Organization