PROJECT III. 3 THIN FILM DEVICES for LARGE AREA ELECTRONICS

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Funding

- Sharp Labs of America grant, 2003 – 2005.
- Two GSRT bilateral Greece-Serbia projects, 2003 – 2007.
- PENED contract, project code 03ED550, 2005 – 2009.
- One postdoctoral fellowship (Dr. Moschou), 2010 – 2012.
- Currently, participation in IMEL cooperation project with Heliosphera (initiation in 2010).

Objectives

The project research objective is the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors (TFTs) fabricated in such films. Such advanced TFTs are necessary for next generation large area electronics systems, which are now in the research and development phase. Specifically, the scientific targets of the project are:

- Evaluation of device parameter hot carrier and irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films with sequential lateral solidification (SLS).
- Investigation of the influence of the crystallization technique and the film thickness on TFT performance, defect densities and degradation for technology optimization.
- Investigation of effects of variations in TFT device structure and in the fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current and noise analysis in ELA TFTs.
- Assessment of material properties of ELA poly-Si TFTs using optical measurements.

On the application level, the project aims at the utilization of these advanced TFTs in the development of novel TFT-addressed displays and microsystems.

MAIN RESULTS IN 2011

Our work during 2011, after conclusion of electrical characterization of single gate thin film transistors and material / optical investigation of polycrystalline silicon films, concentrated in the characterization, degradation and noise investigation of double gate TFTs, fabricated using sequential lateral solidification excimer laser annealing.

Task 1 Characterization of double gate SLS ELA TFTs

Advanced polycrystalline silicon thin film transistors, such as devices fabricated at very low temperatures using sequential lateral solidification excimer laser annealing techniques, are essential for large area electronics and high performance flat panel displays. The objective of this task is the characterization of poly-Si TFTs having various technologically important structures and crystallized with different SLS ELA variations, as well as the determination of process parameters that affect device performance. We have studied the effect of the TFT active region film microstructure, relating the film characteristics themselves with the electrical performance and reliability characteristics of the TFTs. During 2011 we focused on the investigation of double gate TFTs; the presence of a second gate in advanced SLS ELA polysilicon TFTs offers additional possibilities, which cannot be realized with standard top or bottom gate devices, such as the control of TFT electrical parameters by appropriately biasing the bottom gate. Our aim is to

determine the role of both gate lengths on TFT performance and electrical characteristics, probing possible short channel effects.

We characterized TFTs with the same bottom gate length L_{bottom} = 4 μm and channel width W = 16 μm. The top gate length L_{top} varied from 0.5 μm to 4 μm. In Fig. 1 we can see the threshold voltage V_{th} values extracted from the I_{ds}-V_{gt} characteristics, for all top gate lengths L_{top} and bottom gate biases V_{gb} from –3 V to 3 V. As we can observe, there is an almost linear relationship between V_{th} and V_{gb}, as predicted by physical models for SOI MOSFETs with symmetrical top and bottom gate lengths. We also see that by increasing the top gate length, the threshold voltage also increases. This trend can be attributed to the increase of grain boundary traps as the channel length increases, since more grain boundaries and sub-boundaries will be present.

This explanation is further supported by the evolution of $V_{g,max} – V_{th}$, also shown in Fig 1, for increasing channel length. We have previously shown that this difference is directly proportional to the grain boundary trap density; therefore its increase indicates the increase of these traps with channel length, which is consistent with the increase of V_{th} with increasing channel length. Also, for all devices we observe an increase of $V_{g,max} – V_{th}$ with increasing V_{gb}. This is reasonable, as the increase of the bottom gate bias forces the current carriers deeper in the poly-Si active layer, thus "seeing" more traps. More traps are expected to be present as we go deeper, since in previous work we have shown the superiority of the top interfaces compared to the bottom ones.

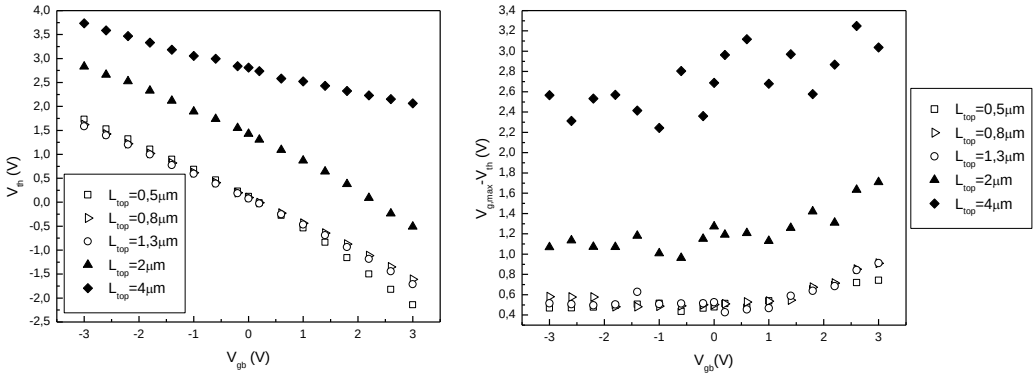

Fig. 1. *Threshold voltage V_{th} (left) and $V_{g,max} – V_{th}$ (right) variation versus bottom gate bias V_{gb} for different top gate lengths, with W = 16 μm and L_{bottom} = 4 μm.*

In order to verify that the trends observed are attributed solely to the top channel length (i.e., that we actually see short channel effects relevant to top gate operation) and not to the variation of the top to bottom length ratio L_{top}/L_{bottom}, we also characterized double gate structures with a set top gate length L_{top} = 2 μm and channel width W = 8 μm and the bottom gate length as a variable. In this case, the ratio L_{top}/L_{bottom} changes through L_{bottom} variation, not through L_{top}; thus there is no channel shrinking and any effects on device parameters extracted from I_{ds}-V_{gt} characteristics can be attributed solely to the L_{top}/L_{bottom} variation. This way we are able to distinguish the two factors that affect the device performance: short channel effects and L_{top}/L_{bottom} variation.

Indeed, in Fig. 2 we observe only a small V_{th} variation (slight increase) as L_{top}/L_{bottom} decreases. On the contrary, in our previous analysis we saw a significant V_{th} decrease with decreasing L_{top}/L_{bottom}. Therefore, our previous observations seem to be independent from any L_{top}/L_{bottom} effects and can mainly be attributed to short channel effects. The same observations can also be made in Fig. 2 for the $V_{g,max} – V_{th}$ variation with L_{top}/L_{bottom}; as L_{top}/L_{bottom} decreases, the grain boundary trap density slightly increases, contrary to the trend in Fig. 1, where we varied the top gate length only.

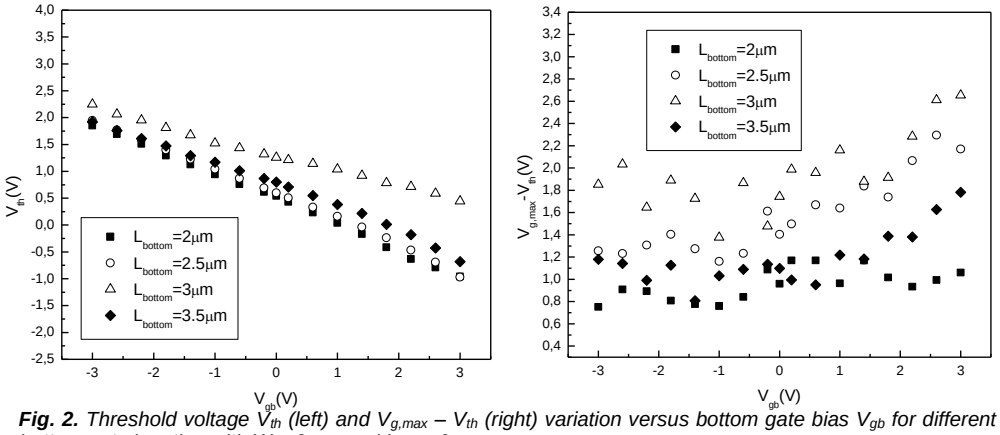

Fig. 2. *Threshold voltage V_{th} (left) and $V_{g,max} - V_{th}$ (right) variation versus bottom gate bias V_{gb} for different bottom gate lengths, with W = 8 μm and L_{top} = 2 μm.*

Summing up, a significant V_{th} increase is observed with increasing top gate length in double gate TFTs and is attributed to the larger number of grain boundaries included in larger channels. This is also indicated by the $V_{g,max} - V_{th}$ increase with increasing L_{top}. The parameter $G_{m,max}$ was not as clearly affected by the channel shrinking, thus indicating that surface scattering of carriers is more important in its determination. We have verified that the observed trends are attributed to short channel effects and not to L_{top}/L_{bottom} variation; the effects of L_{top}/L_{bottom} variation were insignificant compared to short channel effects.

Task 2 Degradation investigation of double gate SLS ELA TFTs

We applied DC stress to double gate TFTs with various top gate lengths L_{top}, channel width W = 8 μm and bottom gate length L_{bottom} = 4 μm. The measured I_{ds}-V_{gt} characteristics after each stress cycle, shown in Fig. 3, indicate that the degradation becomes much more intense for longer channels, although the horizontal electric field is exactly the same as for shorter ones. We believe that this is attributed to the structure of the polysilicon film, since the longer the channel the more grain boundaries and sub-boundaries will be present. The more traps are present within the film the larger the degradation that will occur in the device, due to the extra trap state generation.

The threshold voltage V_{th} evolution with stress time, shown in Fig. 4, indicates that different degradation mechanisms are present for each top gate length. For shorter channels (L_{top} = 0.5 μm) we see only an increase in V_{th} for larger stress times, attributed to hot electron injection. For L_{top} = 0.8 μm we initially observe a small tendency for a V_{th} decrease, indicating minor hole injection, followed by a severe increase, much like for the shorter channel, but at longer stress times. For even longer channels (L_{top} = 1.3 μm) the initial decrease trend is even more intense, followed again by a large increase for long stress times. The fact that the initial hole injection mechanism is only present for long TFT channels and is more intense as the channel is enlarged indicates that it is a channel length dependent degradation mechanism. On the other hand, the electron injection is present for all lengths and is dominant for large stress times in all TFTs. We believe that both mechanisms involve trap generation mainly at the polysilicon interface and not by oxide injection, since we observe a similar picture for the evolution of subthreshold slope S with stress time, also shown in Fig. 4. We see again a clear monotonous behavior only for shorter channel TFTs, while the increase of S (which reflects mid-gap energy level states near the interface) for all devices implies that there occurs mainly mid-gap trap generation near the interface.

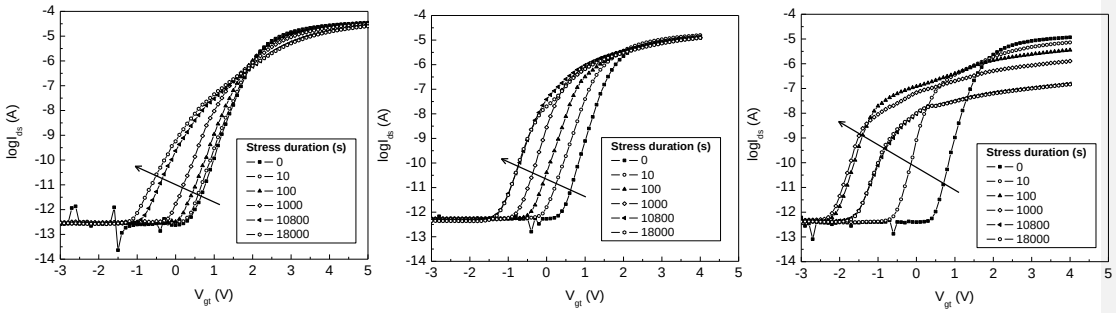

Fig. 3. *I_{ds}-V_{gt} characteristics after successive dc stress cycles for a double gate TFT with L_{top} = 0.5 μm (left), 0.8 μm (middle), 1.3 μm (right).*

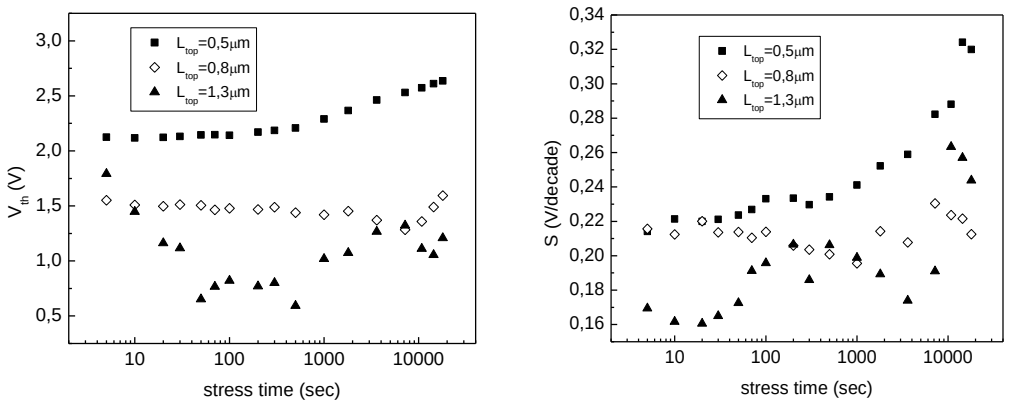

Fig. 4. *Threshold voltage V_{th} (left) and subthreshold swing S (right) evolution with stress time for double gate TFTs of different L_{top} and L_{bottom} = 4 μm.*

On the other hand, the evolution of the maximum transconductance $G_{m,max}$ with stress time, shown in Fig. 5, does not indicate different degradation mechanisms for different channel lengths. For all devices we see a monotonous $G_{m,max}$ decrease, clearly more pronounced for larger length TFTs. This degradation can be attributed to trap generation within the semiconductor, particularly at the channel grain boundaries and sub-boundaries, as indicated by the stress evolution of $V_{g,max} - V_{th}$, also in Fig. 5. This is the parameter we have shown to be directly proportional to the trap density at the grain boundaries and sub-boundaries; thus, the $V_{g,max} - V_{th}$ increase for large stress times reflects an increased trap density and can explain the respective $G_{m,max}$ decrease. Also, we observe a much larger trap generation for the largest channel, thus explaining the much larger $G_{m,max}$ decrease in this case.

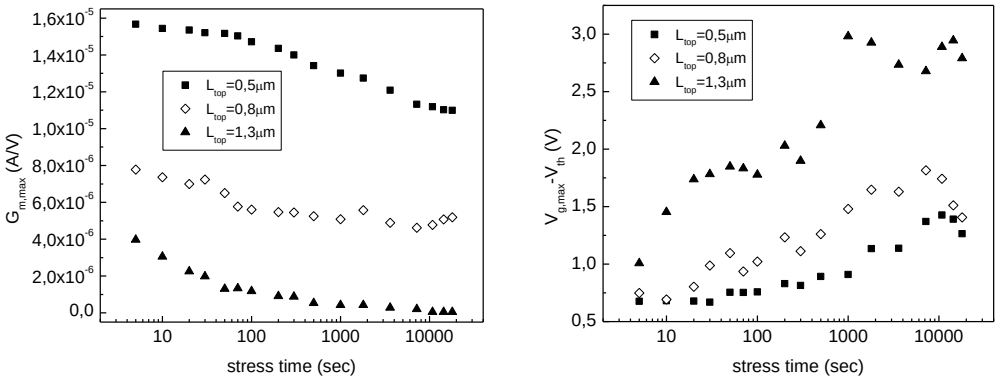

Fig. 5. *Maximum transconductance $G_{m,max}$ (left) and $V_{g,max} - V_{th}$ (right) evolution with stress time for double gate TFTs of different L_{top} and L_{bottom} = 4 μm.*

Task 3 Low frequency noise investigation

The drain current noise power spectral density S_I versus frequency, for sub-micron channel length double gate TFTs was investigated; these measurements were carried out at the University of Thessaloniki, in a project collaboration. Typical plots of the drain current noise power spectral density S_I versus frequency, measured for sub-micron devices (L_{top} = 0.5 μm) before and after stress for time t = 10^4 s, are presented in Fig. 6. Before stress, the spectra exhibit 1/f noise behaviour (flicker noise) in the regions from weak to strong inversion. After stress, they consist of two distinct components: a flicker noise and a Lorentzian noise characterized by a plateau at low frequencies and a fall-off according to $1/f^2$, related to trapping / detrapping processes of carriers at discrete traps, with S_I given by a relation of the form $S_I = A/f + B/(1+(f/f_c)^2)$. The corner frequency f_c is directly related, through the relationship $f_c = 1/2\pi\tau$, to the trap time constant τ characterizing the capture and emission processes of electrons in the traps.

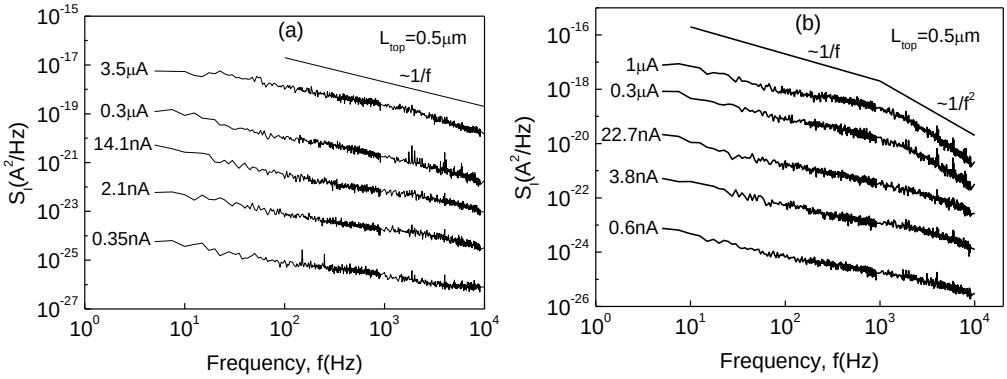

Fig. 6. *Typical noise spectra, measured at drain voltage V_{ds} = 0.1 V and different drain currents in a DG polysilicon TFT with L_{top} = 0.5 μm and L_{bottom} = 4 μm before stress (a, left) and after stressing (b, right).*

The noise spectra of Fig. 6(b) were decomposed to obtain the flicker and the Lorentzian noise components. It is shown that the extracted corner frequency f_c in sub-micron DG TFTs does not change with top gate voltage V_{gt}; this suggests that the trap centres responsible for the observed Lorentzian noise are located in a semiconductor region at some distance from the top gate oxide/polysilicon interface. The physical mechanism of the flicker noise is the variation of the interfacial oxide charge after dynamic trapping and detrapping of free carriers into slow oxide traps at/or near the interface, which leads to surface potential fluctuation and in turn to fluctuations in the inversion charge density. Trapping and detrapping occur through tunneling processes. It has been determined that the normalized noise is increased after stressing, indicating an increase of the interface trap density from 1.2×10^{12} to 2×10^{12} cm^{-2} eV^{-1}.

For the above-micron gate length DG TFT (L_{top} = 1.3 μm), the drain current noise spectra show $1/f^{\gamma}$ behavior (with $\gamma < 1$) both before and after stress (yielding plots similar to 6(a), with a single slope). Generally, if the traps near the interface are distributed uniformly and have uniform energy distribution within the band-gap, they give rise to 1/f spectra; if the interface trap distribution is non-uniform over the oxide, then the noise spectrum frequency dependence deviates from pure 1/f and is approximated as $1/f^{\gamma}$ with $\gamma \neq 1$. For a trap distribution with increasing density towards the interface, there are a greater number of high-frequency traps leading to $\gamma < 1$; similarly, for a trap distribution with increasing density away from the interface, there is a greater number of low-frequency traps leading to $\gamma > 1$.

As shown in Fig. 7, the 1.3 μm unstressed device exhibits an $1/f^{\gamma}$ noise, with γ = 0.65, originating from interface traps with density decreasing with distance into the gate oxide from the top gate interface. However, after stressing the exponent γ increases with increasing gate bias, which implies that the channel carriers, tunneling at a constant energy into the gate oxide, encounter an increasing trap density due to band-bending caused by the gate bias, i.e. the trap concentration becomes higher towards the band edges. This result clearly indicates generation of hot-carrier induced band tail states, related to the distorted-bond defects located at the grain boundaries and sub-boundaries, caused by stressing. The generation of these band tail states can explain the dramatic decrease of the on-state current observed after stressing of long

channel DG polysilicon TFTs, in which a large number of grain boundaries and sub-boundaries are present within the channel. Thus, the overall results obtained from these low frequency noise measurements support the proposed degradation mechanisms of DG ELA polysilicon TFTs with shrinking channel length, as discussed in the Task 2 section.

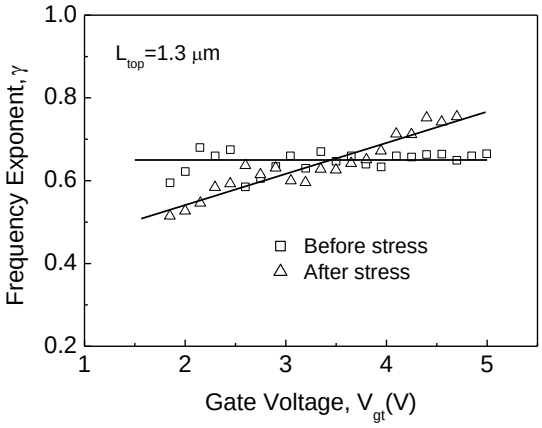

Fig. 7. *Frequency noise exponent against gate voltage for double gate polysilicon TFT with W = 8 μm, L_{top} = 1.3 μm and L_{bottom} = 2.5 μm before and after stressing.*

PROJECT OUTPUT IN 2011

Publications in International Journals

1. "$V_{g,max}$ - V_{th}: A new electrical characterization parameter reflecting the polysilicon film quality of LTPS TFTs", Moschou, D.C., F.V. Farmakis, D.N. Kouvatsos and A.T. Voutsas, Microelectronic Engineering 90, 76, February 2012.
2. "Hydrogen passivation on sequential lateral solidified poly-Si TFTs", Michalas, L., M. Koutsoureli, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, Microelectronic Engineering 90, 72, February 2012.
3. "On the optical properties of SLS ELA polycrystalline silicon films", Moschou, D.C., N. Vourdas, D. Davazoglou, D.N. Kouvatsos, V.E. Vamvakas and A.T. Voutsas, Microelectronic Engineering 90, 69, February 2012.

International Conference Presentations

1. "Short channel effects in double gate polycrystalline silicon SLS ELA TFTs", D.C. Moschou, D.N. Kouvatsos and A.T.Voutsas, to appear in Proceedings of the 28th International IEEE Conference on Microelectronics (MIEL 2012), Nis, Serbia, May 2012.
2. "Trap properties of asymmetrical double gate polysilicon thin-film transistors with low frequency noise in terms of the grain boundaries direction", N. Hastas, A. Tsormpatzoglou, D.N. Kouvatsos, D.C. Moschou, A.T. Voutsas and C.A. Dimitriadis, to appear in Proceedings of the 28th International IEEE Conference on Microelectronics (MIEL 2012), Nis, Serbia, May 2012.
3. "Short channel effects on LTPS TFT degradation", D.C. Moschou, N.A. Hastas, A. Tsormpatzoglou, D.N. Kouvatsos, C.A. Dimitriadis, and A.T. Voutsas, Proceedings of the 8th International TFT Conference (ITC 2012), Lisbon, Portugal, January 2012.
4. "$V_{g,max}$ - V_{th}: A new electrical characterization parameter reflecting the polysilicon film quality of LTPS TFTs", Moschou, D.C., F.V. Farmakis, D.N. Kouvatsos and A.T. Voutsas, Proceedings of the 7th International Thin Film Transistors Conference (ITC 2011), Cambridge, United Kingdom, March 2011.