LOW PRESSURE CHEMICAL VAPOR DEPOSITION (LPCVD) ($TEOS$ and Si_3N_4 Reactor)

MODEL: TEMPRESS

INSTALLATION PLACE: Cleanroom of "Nanotechnology and Microsystems Laboratory", Department of Microelectronics

DESCRIPTION: LPCVD refers to a thermal process used to produce chemical precursors needed to form a semiconductor-grade film on a substrate under low- pressure condition. Deposition of film growth in a LPCVD process can be controlled precisely and accurately. LPCVD is an indispensable element in the semiconductor industry.

SPECIFICATIONS

1. One horizontal LPCVD quartz tube for Si_3N_4 and SiO_2 deposition (furnace A1)
2. SiO_2 deposition
   a) Typical process parameters:
      i) Source: TEOS – TetraEthylOrthoSilicate $Si(OC_2H_5)_4$ (EX-Grade: 99.9999%)
      ii) TEOS flux: 10 – 40 sccm,
      iii) Temperature: 700 – 710 ºC
      iv) Deposition rate: 30 – 80 Å/min
      v) Deposition Pressure: 300mTorr
   b) Substrates: Silicon, III-Vs, other semiconductors, Si_3N_4
3. Si_3N_4 deposition
   a) Typical process parameters:
      i. Source Gases: Ammonia (NH_3) and Dichlorosilane (DCS, SiH_2Cl_2)
      ii. Fluxes : 20 – 60 sccm
      iii. Temperature: 800 – 810 ºC
      iv. Pressure: 200 – 230mTorr
      v. Deposition rate= 30 – 40 Å/min
   b) Deposition substrates: Silicon, III-Vs, other semiconductors, SiO_2
4. Sample size: 3" / 4" wafer and smaller samples
5. Vacuum System: For vacuum ~10 mTorr: i) Booster pump (Booster WAU 251-Leybold), ii) Mechanical oil pump (Leybold D65 BCS)

APPLICATIONS

1. TEOS-SiO_2: Deposited oxide are is extensively in microelectronics devices and MEMS as: gate dielectric, device isolation (Surface-Trench-Isolation), hard-mask against implantation and diffusion, waveguides etc
2. Si_3N_4: Silicon nitride is used extensively in microelectronics devices and MEMS as: gate dielectric, oxidation mask, passivation layer, etch stop, atom diffusion blocker, antireflection coating, membranes, waveguides etc

CERTIFICATION/ACCREDITATION

The facility is not certified or accredited.

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