Project III. 1: MICROMACHINED SILICON SENSORS and MICROSYSTEMS

Project leader: A. G. Nassiopoulou

Other key researchers: C. Tsamis, A. Tserepi, I. Raptis, P. Normand and H. Contopanagos

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Phd students: D. Pagonis, S. Polymenakos

External collaborations: D. Tsoukalas (NTUA), G. Kaltsas (TEI of Athens)

Projects Running:

- EU, IST, IP : Goodfood, contract N^o: 508774
- “Remon Medical”, Industrial cooperation
- Greek-Polish cooperation
- Archimedes (collaboration with TEI of Piraeus)
- Pythagoras (collaboration with the University of Patras)
- Joint project with the University of Cyprus “Photothermal detection of hydrogen”

Main objectives:

- Development of silicon micromachined processes
- Development of novel silicon sensors based on new materials and new processes
- Design, fabrication and testing of microsystems using silicon sensors.

Main results in 2004:

a) Porous silicon technology

Porous silicon is fabricated on a silicon wafer by electrochemical dissolution of bulk silicon. It may be formed locally on a silicon substrate as a thin or thick membrane, through a masking layer.

Due to the porous structure of the material, it provides thermal and electrical isolation and it may be used in different sensor applications.

a_1) Porous silicon-sealed microchannels in silicon

D. N. Pagonis, G. Kaltsas and A. G. Nassiopoulou

An electrochemical process has been developed for the fabrication of sealed air cavities and capped microchannels of different designs on a silicon wafer. The capping material is a porous silicon membrane which is planar to the silicon substrate. Two interesting applications of this technology are targeted: a) The effective local thermal isolation on a silicon wafer for use in micromachined thermal sensors, b) The potential use of this technology in the fabrication of microfluidic devices. An example of a microchannel in silicon sealed with porous silicon is shown in *fig. III.1.1*

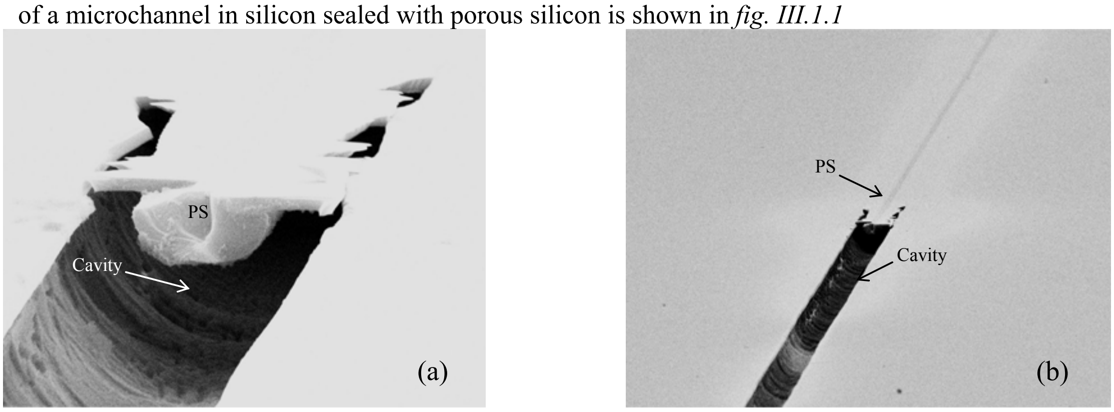

Fig. III.1.1: *Top view SEM images of a microchannel in a silicon wafer, sealed with porous silicon. In both (a) and (b) the porous silicon sealing has been partially removed in order to uncover the channel‘s inner surface.*

a_2) Porous silicon micro-hotplate technology

D. N. Pagonis, G. Kaltsas and A. G. Nassiopoulou

An improvement of porous silicon technology for local thermal isolation on bulk crystalline silicon has been achieved in 2004. The technique used consists of forming an air cavity below the porous layer to increase the thermal isolation efficiency (*fig. III.1.2)*. Both porous silicon and the cavity underneath are formed during the same electrochemical process in two steps: in step 1 the current density used is below a critical value, and in step 2 it is switched to a value above the critical current for electropoliching. In this way, porous silicon is formed first, followed by the formation of the cavity underneath. An SEM image of such structure is shown in *fig. III.1.3.*

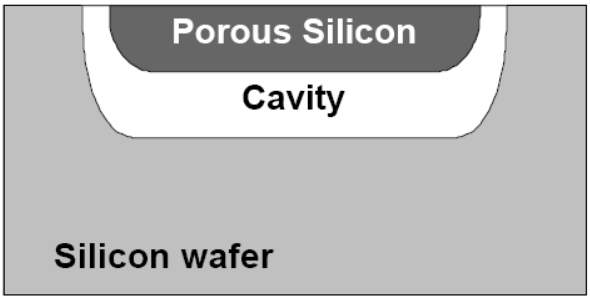

Fig. III.1.2: *Schematic presentation of the isotropic formation of the cavity. Due to the isotropic process, silicon etching occurs under the PS membrane and also under the surrounding mask, resulting in degredation of the membrane. To overcome this effect, a detailed study on the nature of the masking layer was performed to constrain silicon etching underneath the surrounding masking layer.*

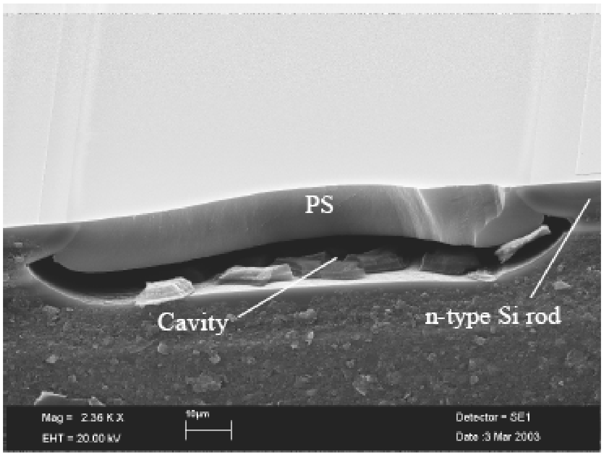

Fig. III.1.3: *SEM image of a cross section of a porous silicon freestanding membrane with a cavity underneath.*

b) Chemical Sensors

i. Metal Oxide Sensors

b.i.1. Optimization of micro-hotplates for low power chemical sensors-Characterization at reduced pressures

K. Spyropoulou and C. Tsamis*

(MSc graduate student)*

One major requirement for the fabrication of low power sensors, especially for integration in arrays, is the reduction of thermal losses. This can be achieved by the fabrication of the active elements of the sensors on suspended structures (micro-hotplates). Two different types of micro-hotplates have been used in the literature: The closed-type membrane, where the membrane overlaps the silicon substrate along its periphery and the suspended-type membrane, where the membrane is supported on the Si substrate by means of supporting beams. In the latter case, the thermal losses to the substrate take place only through the supporting beams, and thus they are minimized compared to the closed type membrane.

During this year, we performed a systematic study of various thermal isolation techniques. Combined experimental and simulation results using Coventorware *(Fig. III.1.4)* were used in order to estimate material properties such as thermal conductivity and to optimize micro-hotplate design. Measurements were performed at reduced pressures in order to minimize the parameters involved during modeling and to achieve better estimation of the thermal conductivity. For sufficiently low pressures, thermal losses in air can be minimized and thus ignored during the analysis of the *results (Fig. III.1.5).* As an example, two different isolation techniques, one using a thick porous silicon layer directly grown on the silicon substrate and the other using a thin suspended porous silicon micro-hotplate, were evaluated. A unique value of PS thermal conductivity was estimated and it was found to fit the experimental results for the different sensor designs that were characterized.

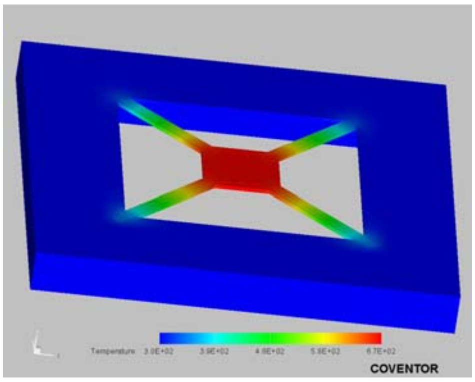

Fig. III.1.4: *Temperature distribution of a suspended micro-hotplate, as predicted by Coventorware*

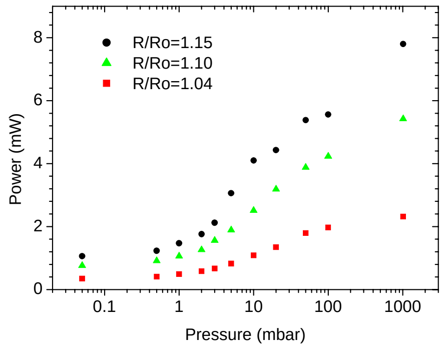

Fig. III.1.5: *Power required to maintain the same change of the heater resistance (and thus the temperature) as a function of the ambient pressure.*

b.i.2 The influence of thermal treatment on the stress characteristics of suspended Porous Silicon membranes on silicon

D. Papadimitriou, C. Tsamis and A. G. Nassiopoulou*

(SEMFE/NTUA)*

Over the last years, porous silicon (PS) has attracted significant interest, due to its potential usage in various fields of applications. PS layers have been effectively used for local thermal isolation on bulk silicon and as materials of suspended micro-hotplates for low power thermal sensors. Optimization of the mechanical properties of PS layers as well as stress control is a main issue that has to be considered for most of these applications.

During this year, we investigated in a systematic way the evolution of the stress that develops in PS layers as a function of porosity and thermal treatment for various micro-hotplate designs *(fig. III.1.6)*. Micro-Raman spectroscopy was used for stress characterization in two cases: (a) for supported and (b) for suspended PS layers *(fig. III.1.7)*. Stress-analysis based on these spectra reveals that membranes treated in an inert ambient, at moderate temperatures, are less strained and do not break when they are released from the substrate. The information obtained is useful for optimizing the fabrication process and the design of the devices.

Fig. III.1.6: *Fully released porous silicon micro-hotplate used as test structure for the stress measurement. The thickness of the membrane is 4 μm.*

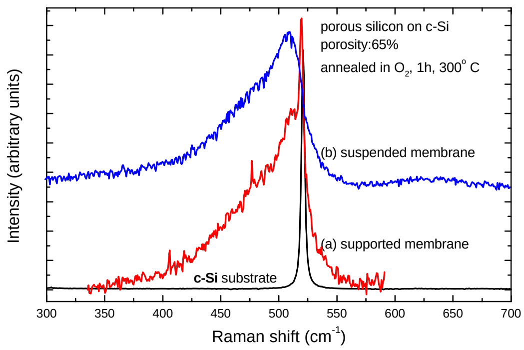

Fig. III.1.7: *Raman spectra of (a) supported and (b) suspended PS membrane of porosity 65% after annealing at 300°C for 1h in O_2 ambient. A spectrum of the c-Si substrate is also shown.*

b.i.3. Control Circuit Design for MOX sensors

S. Chatzandroulis, D. Tassopoulos, P. Roubogiannakis and C. Tsamis

This activity includes the design of the control and reading electronics for metal oxide chemical sensors. MOX sensors consist of a heater resistance R_h and a chemically sensitive resistance R_s. The interface has to operate in a wide resistance range which could be between 300 Ohms and 20 Mohms, depending on the catalytic material used. Furthermore, it should be able to operate with sensor heaters made either of Pt or polysilicon. An electronic board, able to handle up to 4 sensors, has been implemented using discrete components. For the measurement of the sensitive resistance, Rs is placed in a voltage divider with selectable range resistors and is periodically sampled by the microcontroller ADC. Then the Rs value is calculated on the AVR and transmitted to the PC via the RS232. To drive the heater to the required temperature, a dedicated power circuit, which is controlled from the PWM output of the microcontroller, is used. To regulate the heater temperature, the heater resistance R_h is sampled periodically by the AVR which then decides to either increase or decrease the PWM output. *Fig. III.1.8* shows the above electronic circuit using discrete components.

Furthermore, an ASIC containing all of the analog electronics necessary to control and read 4 MOX sensors is under development.

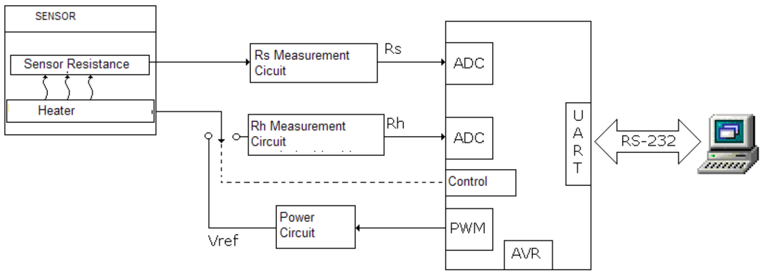

Fig. III.1.8: *MOX Control and Reading Circuit using discrete components.*

b.ii. Bimorph Chemical Sensors

b.ii.1. Design and Fabrication of Bimorph Chemical Sensors

S. Chatzandroulis, D. Goustouridis, J. Fraggakis, S. Polymenakos, I. Raptis, D. Tsoukalas (SEMFE/NTUA) and P. Normand*

(MSc graduate student)*

The activity aims at the development of a bimorph chemical sensor array for use in aroma recognition in e-nose applications. To this end, a new technology based on the bending of single-crystal silicon/polymer bilayers for the fabrication of selective chemical sensors, has been developed. The device utilizes a thin silicon microstructure, which could be a thin Si membrane or cantilever, covered by polymers like PMMA, PHEMA, PVAc, EPN etc, as chemical sensing layers. Of special interest, in this respect, were patternable polymer materials (e.g. PMMA, PHEMA), since the use of such materials facilitates the construction of bimorph chemical arrays. When the device is exposed to a volatile organic compound (VOC) concentration (e.g. methanol, ethanol) the overlying polymer swells forcing the silicon microstructure to bend and approach the substrate. This bending is then detected as a capacitance change in function with VOC ambient concentration.

Optimization of initial devices has followed two routes: one focusing on the geometric characteristics of bimorph sensors and one focusing on the understanding of polymer/analyte kinetics and swelling properties. For the first activity, extensive simulations of cantilever type devices have been performed using Coventorware® *(fig. III.1.9)*. Cantilevers of various lengths (ranging from 100μm to 2500μm) have been studied and a finite element (FE) model has been developed to facilitate the design and optimization of these devices. Experimental behavior is approximated by taking into account the stress induced in the cantilever due to the polymer swelling *(fig. III.1.10)*. Simulation results are in good agreement with experimental values.

Furthermore, within the second activity, a new method has been developed to engineer PHEMA swelling properties using controlled deep UV exposures. The new method allows for the modification of sensor sensitivity using this polymer.

b.ii.2. Polymer Materials for Chemical Sensors

D.Goustouridis, S.Chatzandroulis, K.Manoli, M.Sanopoulou (IPC) and I.Raptis*
(MSc graduate student)*

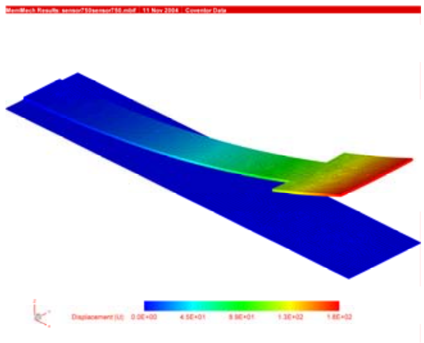

Fig. III.1.9: *FE model: Displacement of the Si/polyimide bimorph cantilever.*

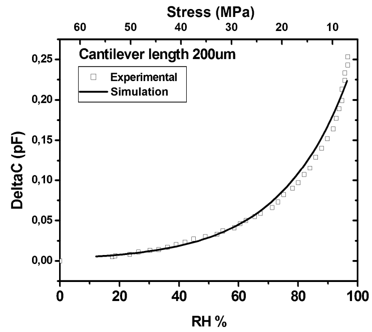

Fig. III.1.10: *Comparison between simulated and experimental data for a 200 μm long cantilever*

Optimization of bimorph chemical sensors relies, in great part, on the understanding of the physicochemical properties of the chemically sensitive materials deposited onto the micromechanical silicon structure. To this end, a new white light interferometric experimental setup has been developed *(fig. III.1.11)*. The setup is built around a chamber where controlled concentrations of volatile organic compounds may be introduced and allows the in-situ measurement of polymer layer thickness during analyte exposure with better than 0.5nm accuracy. The research focused on two well known polymer materials: PHEMA and PMMA. The two materials exhibit different, normalized to thickness, expansion to various volatile organic compounds, depending on the combination of the polarity and hydrogen bonding capability of the analyte. A wide polymer film thickness (50 and 600nm) range was examined and it was revealed that the normalized film expansion in both PHEMA and PMMA is nearly constant for films thicker than 100nm and increases for thinner films.

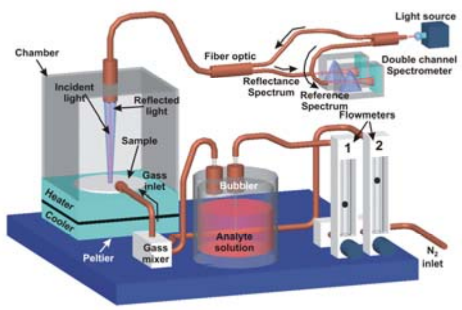

Fig. III.1.11: *Polymeric film characterization apparatus.*

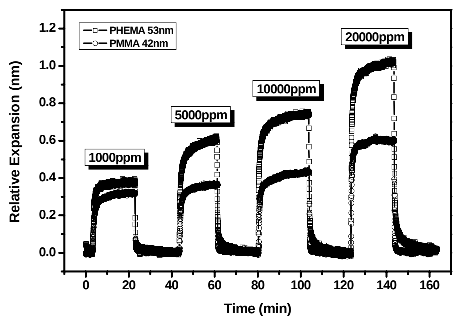

Fig. III.1.12: *Film thickness evolution vs. methanol vapor concentration for PHEMA, PMMA.*

Also within this activity a new methodology to engineer the swelling properties of PHEMA using UV irradiation has been discovered *(fig. III.1.13)*. The new methodology allows for the modification of sensor sensitivity and aims at the construction of diversified chemical bimorph arrays using just one polymer.

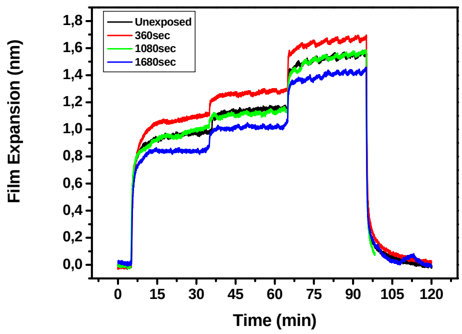

Fig. III.1.13: *Swelling behavior of four PHEMA films (140nm) treated with different DUV exposure conditions as a function of methanol concentration (0, 5000, 10000 and 20000ppm)*

c) Capacitive-type Micromechanical Silicon Sensors

D. Tsoukalas, S. Chatzadroulis, D. Goustouridis and P. Normand

During 2004 the industrial cooperation in the field of pressure sensors was carried on by completing the delivery of a first order of 10.000 units and the development of a new improved version of the device according to new specifications.

Also in 2004 the patent application to USPTO came to an agreeable end by the issue of U.S patent no 6,704,185. The procedure is also in progress in other countries.

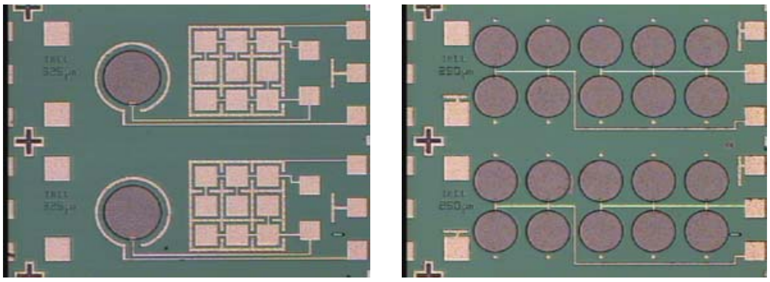

Fig. III.1.13: Capacitive type silicon sensors

d) Porous silicon CMOS-compatible on-chip resonators

H. Contopanagos and A. G. Nassiopoulou

A comprehensive approach for designing on-chip resonators using low-loss porous-silicon technology has been developed. We have focused on technology parameters that can be integrated within a standard CMOS process, such as a 0.13 micron CMOS and have targeted optimization of fundamental RF building blocks of direct interest to wireless communications chips.

First, we have designed optimized on-chip inductors with maximized quality factors, using electromagnetic simulations based on Method-of-Moment or Finite-Elements computer codes to obtain the optimum metallization for minimizing physical loss and maximizing the quality factors. In general, we predict a quality factor enhancement of about a factor of 2 when using porous Si, relative to standard CMOS of same metal thickness. These calculations were performed assuming certain electrical characteristics of porous Si as reported in the literature. The enhancement is due to both, shielding of the lossy Si substrate achieved by a thick porous silicon layer, and custom metal design of the inductor relative to standard designs found in the literature. In the future we will make these prototypes on porous silicon fabricated and electrically characterized at IMEL, and we will use those material parameters for the designs presented here.

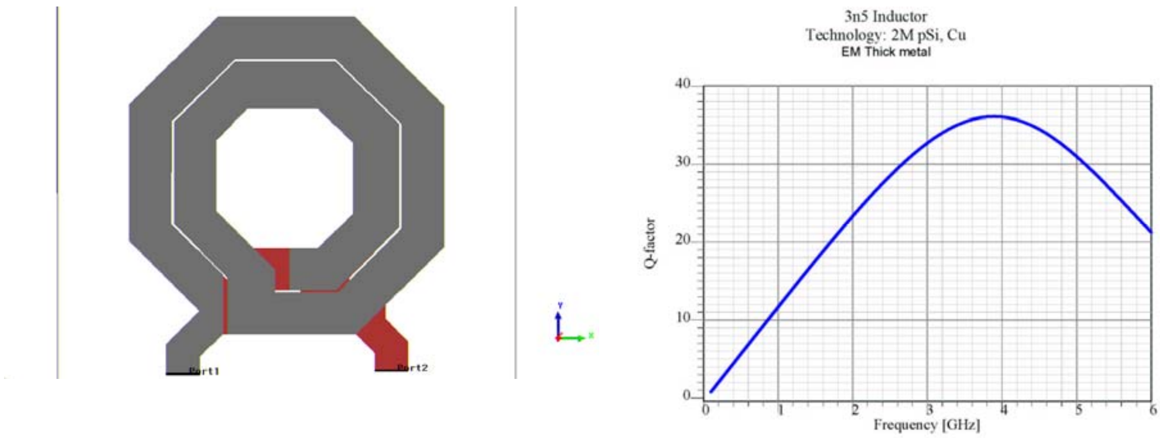

Fig.III.1.14: *2-metal-layer optimized inductor design on porous-Si for an inductance value L=3.5 nH and its predicted quality function in microwave frequencies for Bluetooth/WLAN systems.*

Second, we have synthesized more complicated systems, and in particular pass-band filters integrated on-chip, using the previous high-Q inductors. Traditional passive LC filters can not be realized on standard CMOS technology because of the loss created by the Si substrate, in addition to the metal losses. Other difficulties with on-chip realizations, in addition to the losses, derive from the high-frequency coupling of each filter element to the substrate and from the parasitic electrical quantities developed in lay-out at the scale of CMOS technologies for RFICs. We dissect these physics and design issues and show how one can synthesize successfully on-chip filters on a low-loss porous-Si substrate which can be included in a standard process flow in CMOS. We quantify, feed back into the design and optimize all quantities produced by the material lay out and physical properties of this technology. This year's results appear promising in arriving at completely passive on-chip filters. If these are successfully realized, they will not suffer from the substantial noise problems that plague active integrated filter solutions currently available.

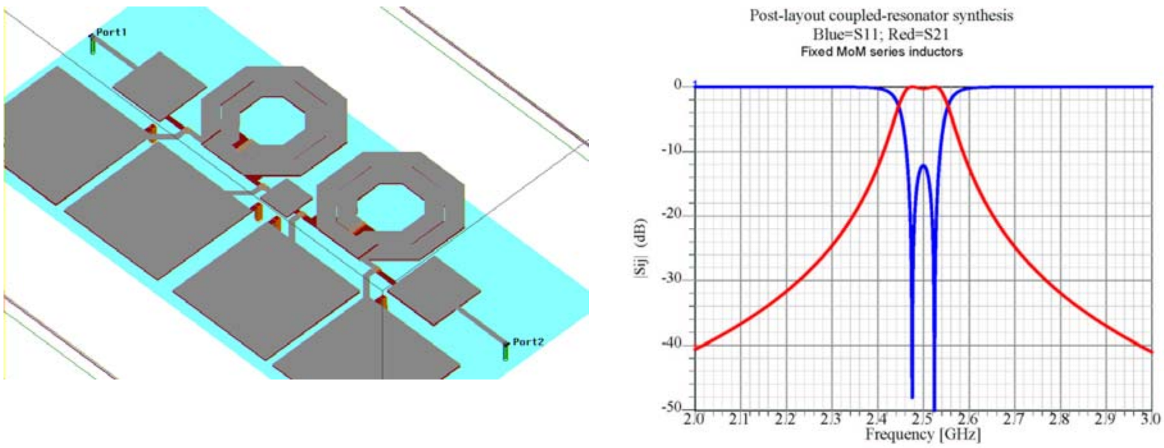

Fig.III.1.15: *Simulated Bluetooth passive pass-band filter layout based on coupled resonator synthesis and post-layout response (with only reactive parasitics extracted).*

Work in progress involves efficient simulation of the complete filter block with all losses present and fabrication and characterization of materials and prototypes based on above synthesis results.

Finally, 3 U.S. patents were issued in 2004 on inventions related to the above topics, see **PATENTS.**

PUBLICATIONS in INTERNATIONAL JOURNALS

1. "Capacitive Type Chemical Sensors Using Thin Silicon/Polymer Bimorph Membranes", S. Chatzandroulis, E. Tegou, D. Goustouridis, S. Polymenakos, D. Tsoukalas, Sensors and Actuators B: Chemical, Volume 103, Issues 1-2, 29 September 2004, Pages 392-396
2. "Fabrication of Chemical Sensors based on Si/polymer bimorphs", S. Chatzandroulis, E.Tegou, D. Goustouridis, S. Polymenakos, D. Tsoukalas, Microelectronic Engineering, Volumes 73-74, June 2004, Pages 847-851
3. "Polymeric film characterization for use in Bimorph Chemical Sensors", S.Chatzandroulis, D.Goustouridis, I.Raptis, accepted for publication in Microelectronic Engineering
4. "Characterization of Polymer Layers for Silicon Micromachined Bilayer Chemical Sensors Using White Light Interferometry", D. Goustouridis, K. Manoli, S. Chatzandroulis, M. Sanopoulou, I. Raptis accepted for publication in Sensors and Actuators B
5. "The influence of thermal treatment on the stress characteristics of suspended Porous Silicon membranes on silicon", D. Papadimitriou, C. Tsamis and A. G. Nassiopoulou, Sensors and Actuators B: Chemical, Volume 103, Issues 1-2, Pages 356-361 (2004)
6. "Fabrication and testing of an integrated thermal flow sensor employing thermal isolation by a porous silicon membrane over air cavity", D. N. Pagonis, G. Kaltsas, and A. G. Nassiopoulou, J. Micromech. Microeng. 14, 1-5, 793-797 (2004)
7. "The influence of thermal treatment on the stress characteristics of suspended porous silicon membranes", D. Papadimitriou, C. Tsamis and A. G. Nassiopoulou, Sensors & Acruators B, 103, 356-361, (2004)
8. "Porous silicon membranes over cavity for efficient local thermal isolation on silicon for application in Si thermal sensors", D. N. Pagonis, A. G. Nassiopoulou and G. Kaltsas, J. Electrochem. Soc. 151 (8) H 174-H179 (2004)
9. "Gas flow meter for applications in medical equipment for respiratory control-Study of the package and housing" G. Kaltsas and A. G. Nassiopoulou, Sensors & Acruators A, 100, 413-422 (2004)

PRESENTATIONS in CONFERENCES

1. "Combination of integrated thermal flow and capacitive pressure sensors for high sensitivity flow measurements in both laminar and turbulent regions", G. Kaltsas, D. Goustouridis, A. G. Nassiopoulou and

D. Tsoukalas, *Journal of Physics*: Conference Series (accepted for publication), *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*

2. "A microcontroller-based interface circuit for data acquisition and control of a micromechanical thermal flow-sensor", P. Asimakopoulos, G. Kaltsas and A. G. Nasisopoulou, International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004), November 14-17, Athens, Greece, *To appear in Journal of Physics: Conference Series*
3. "Simultaneous use of flow and pressure sensors for flow determination in both laminar and turbulent regions", G. Kaltsas, D. Goustouridis, A. G. Nassiopoulou and D. Tsoukalas, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*, November 14-17, Athens, Greece
4. "Investigation of different operation modes of a micromechanical thermal flow sensor, using a microcontroller-based interface circuit", P. Asimakopoulos, G. Kaltsas and A. G. Nassiopoulou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004),* November 14-17, Athens, Greece
5. "Stress characteristics of suspended Porous Silicon microstructures on silicon", K. Anestou, D. Papadimitriou, C. Tsamis and A.G. Nassiopoulou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*, November 14-17, Athens, Greece
6. "A CMOS compatible thermal accelerometer without solid proof mass, based on porous silicon thermal isolation", G. Kaltsas, D. Goustouridis and A. G. Nassiopoulou*, IEEE Sensors 2004*, Vienna, Austria, October 24-27, 2004
7. "A CMOS compatible process for porous silicon/air cavity formation for application in thermal sensors and microfluidic devices", D. N. Pagonis, A. G. Nassiopoulou and G. Kaltsas, *4th Int. Con. 4th Int. Con. On Porous Semiconductors Science and Technology (PSST 2004)*, Cullera-Valencia, Spain, March 14-19, 2004
8. "Porous silicon micro-hotplates for low power thermal sensors. Measurements at reduced pressures and estimation of porous silicon thermal conductivity of porous silicon", C. Tsamis, K. Spyropoulos and A.G. Nassiopoulou, *4th Int. Con. On Porous Semiconductors Science and Technology (PSST 2004)*, Cullera-Valencia, Spain, March 14-19, 2004
9. "Fabrication and characterization of an integrated thermal flow sensor using porous silicon membranes over cavity for local thermal isolation", D. N. Pagonis, A.G. Nassiopoulou and G. Kaltsas, applied to the *XX Panhellinion Conference on Solid State Physics and Materials Science26-29 September*, Ioannina 2004
10. "Characterization of Polymer Layers for Silicon Micromachined Bilayer Chemical Sensors Using White Light Interferometry", D. Goustouridis, S. Chatzandroulis, M. Sanopoulou, I. Raptis, *EUROSENSORS XVIII, September 13-15, 2004 - Italy - Rome*
11. "Polymeric film characterization for use in Bimorph Chemical Sensors", S. Chatzandroulis, D. Goustouridis, I. Raptis, *Micro- and Nano-Engineering (MNE) 2004, Rotterdam, The Netherlands, September 19 - 22*
12. "Modification Of Polymer Swelling By UV Irradiation For Use In Chemical Sensing", D. Goustouridis, S. Chatzandroulis, I. Raptis, E.S. Valamontes, *IEEE SENSORS 3rd Int. Conference on Sensors, Vienna, Austria, Oct. 24-27, 2004*
13. "Simulation of Capacitive type Bimorph Humidity Sensors", J. Fragakis, S. Chatzandroulis, D. Papadimitriou, C. Tsamis, "MMN 2004, 15-17 November 2004 - Athens, Greece
14. "Polymeric film characterization for use in bimorph chemical sensors", S. Chatzandroulis, D. Goustouridis, I. Raptis, MMN 2004, 15-17 November 2004 - Athens, Greece
15. "Porous silicon micro-hotplates for low power thermal sensors. Measurements at reduced pressures and estimation of porous silicon thermal conductivity", C. Tsamis, K. Spyropoulou and A. G. Nassiopoulou, *4th International Conference on "Porous Silicon Science and Technology", PSST 2004, March 2004, Valencia, Spain* ***(Oral presentation)***
16. "Stress characteristics of suspended Porous Silicon microstructures on silicon"K. Anestou, D. Papadimitriou, C. Tsamis and A. G. Nassiopoulou, *2nd Conference on Microelectronics, Microsystems, Nanotechnology, MMN 2004, 15-17 November 2004, Athens, Greece* ***(Poster presentation)***
17. "Wheeler's law and related issues in Integrated Antennas", H. Contopanagos, S. Rowson and L. Desclos, published in 2004 *IEEE Antennas and Propagation Society International Symposium Digest*, (June 20-26, 2004, Monterey, CA).
18. "Electromagnetic design methods in systems-on-chip: Integrated filters for wireless CMOS RFICs" H. Contopanagos, to appear in *Journal of Physics: Conference Series*, *International Conference on Microelectronics, Microsystems and Nanotechnology* (MMN 2004, November 14-17, Athens, Greece).

INVITED TALKS

1. "Porous silicon for sensor applications", A. G. Nassiopoulou, **Invited talk**, NATO Advanced Study Institute on Nanostructured and Advanced Materials for Optoelectronic, Photovoltaic & Sensor applications, Sozopol, Bulgaria, September 6-17, 2004
2. "Electromagnetic design methods in systems-on-chip: Integrated filters for wireless CMOS RFICs" H. Contopanagos, **Invited talk,** International Conference on Microelectronics, Microsystems and Nanotechnology *(MMN 2004, November 14-17, Athens, Greece).*

Msc THESES

K. Spyropoulou, "*Modeling and optimization of micro-hotplates for thermal sensor applications*" (Msc Course in Microelectronics, Univ. of Athens, Responsible: C. Tsamis)

PATENTS

1. U.S patent N^{o} 6,704,185, Mar. 9, 2004, “Capacitive Pressure Responsive Devices and Their Fabrication”
2. US Patent N^{o} 6,812,544 November 2, 2004, “Integrated circuit having oversized components”, H. Contopanagos and C. Komninakis
3. US Patent N^{o} 6,809,623 October 26, 2004, “High Q on-chip inductor”, S. Kyriazidou, H. Contopanagos and R. Rofougaran
4. US Patent N^{o} 6,709,977 March 23, 2004, “Integrated circuit having oversized components and method of manufacture there of ”, H. Contopanagos and C. Komninakis