Project II. 1: SEMICONDUCTOR NANOSTRUCTURES: SCIENCE & APPLICATIONS

Project leader: Dr A. G. Nassiopoulou

Other key researchers: V. Ioannou-Sougleridis, E. Tsoi, P. Normand and N. Papanikolaou

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Projects Running:

- EU IST FORUM FIB, Contract N°: 29573
- EU IST FET ESCHER, Contract N°: 33287
- EU NoE IST SINANO, Contract N°: 506844

Main objectives:

- Fabrication and characterization of semiconductor nanostructures (quantum wires, quantum dots, optical properties, charging effects, self-assembling, ordering)
- Application in non-volatile memories
- Self-assembled building blocks for nanoelectronics (self-assembly of nanoparticles, ordering on microcrystals, application in nanoelectronic devices, transport properties)
- Calculation of heat transport in the nanoscale with molecular dinamics

Mail results in 2004:

a) Two-demensional arrays of ordered, highly dense and ultra small Ge nanocrystals in thin SiO_2 layers

A. Olzierski, E. Tsoi and A. G. Nassiopoulou

In this work, we have developed, in collaboration with ISI/FZJ Julich and $CRMC_2$-CNRS-Marseille, two original processes for the fabrication of 2-dimensional arrays of ordered Ge nanocrystals embedded in thin SiO_2 layers for their use in nanocrystal floating gate memories. Ordering is achieved by a combination of focused ion beam nano-patterning and self assembly of Ge islands on the patterned SiO_2 surface. In the first process the Ge islands are grown by selective chemical vapor deposition of Si / Ge / Si on Si holes fabricated by FIB patterning, while the second process uses solid phase epitaxy by MBE of amorphous Ge on SiO_2 at room temperature, followed by annealing for crystallization. Highly ordered and highly dense ($1.5\times10^{11}/cm^2$) ultra-small (~ 20 nm) Ge dots on SiO_2 were achieved by both processes. Examples are given *in fig. II.1.1* This work has been carried out within the European IST project FORUM FIB: Fabrication, Organisation and Use of Memories obtained by Focused Ion Beam.

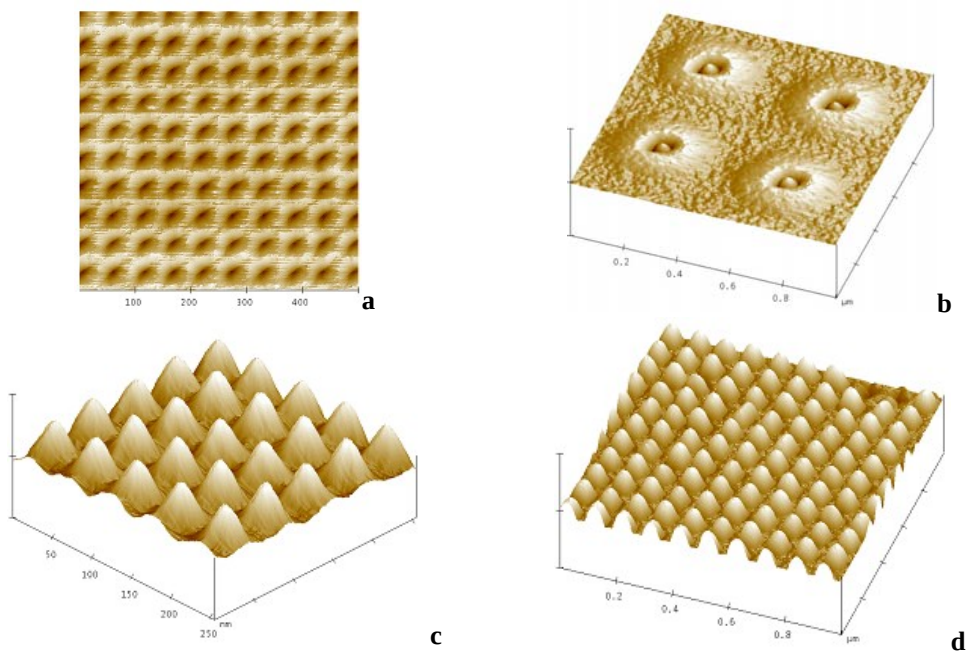


Fig. II.1.1*: AFM images of a regular array of FIB holes with diameter of about 40 nm before (a) and after (b) the deposition of Si/Ge/Si stack. (c) and (d) show the perfectly uniform 2D dot arrays after oxide removal in an area of 250 x 250 nm^2 and 1x1 μm^2 respectively.*

b) 2-D Silicon nanocrystal layers within SiO_2 by LPCVD deposition of amorphous silicon, followed by solid phase crystallization and thermal oxidation.

E. Tsoi, A. Salonidou, V. Ioannou-Sougleridis, P. Normand, and A. G. Nassiopoulou

Silicon nanocrystals memory cells of an n-MOSFET type were fabricated and tested, based on a silicon nanocrystal gate MOS structure fabricated by low-pressure chemical vapor deposition (LPCVD) of amorphous silicon (α-Si) on a tunneling silicon dioxide layer, followed by solid phase crystallization and high temperature thermal oxidation. A layer of silicon nanocrystals embedded in SiO_2 at a tunneling distance (3.5nm) from the silicon substrate was thus formed. The obtained memory cells showed a full-write, full-erase memory window of the order of 0.5V under charging with pulses of 7V and -8V respectively at 100 ms.

The influence of oxide traps (located near the Si substrate-tunnel oxide interface) on the charging characteristics of Si-nanocrystals embedded within SiO_2 layers were investigated by monitoring the admittance characteristics at room temperature. In the samples investigated, an oxide hole trap located almost at the Si-SiO_2 interface of the silicon substrate, having a distribution of energy states, has been detected, which controls the hole injection and transfer to the Si nanocrystals. Upon capturing a hole the defect energy levels undergo a transition due to lattice relaxation effects and hole charging of the Si-nanocrystals occurs via an inelastic two-step tunneling mechanism. High temperature annealing was found to reduce the density of these near-interfacial defects, therefore reducing the coupling between the Si-nanocrystals and the substrate.

c) Very thin porous alumina films on silicon for use as templates for nanofabrication

M. Kokonou and A. G. Nassiopoulou

By anodizing thin aluminum films on Si in sulfuric or oxalic acid aqueous solutions, we get anodic alumina films with ordered cylindrical vertical pores, arranged in a hexagonal close-packed structure. The diameter of the pores is in the range of 10 to 100 nm, depending on the electrochemical solution used.

In this work, very thin anodic alumina films were fabricated, with thickness down to ~10 nm. These films may be used as templates for the fabrication of arrays of quantum wires or dots for use in nanoelectronic devices.

By monitoring the anodization time it is possible to fabricate ordered SiO_2 nanodots at the bottom of each vertical pore (at the interface of alumina with silicon). By dissolving the alumina film, a 2-D array of SiO_2 nanodots is obtained. This patterned Si-SiO_2 surface is very appropriate for the growth of ordered 2-D arrays of silicon nanocrystals.

Fig. II.1.2 shows AFM images of SiO_2 nanodots on silicon, fabricated through an alumina template.

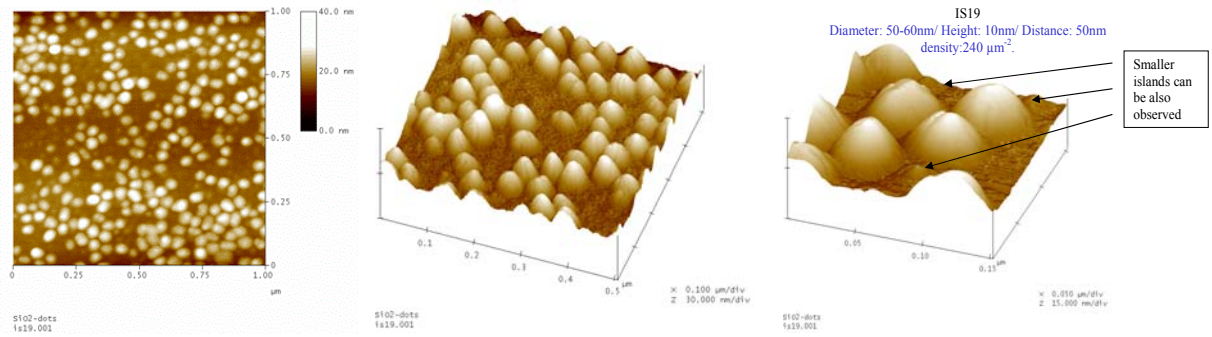


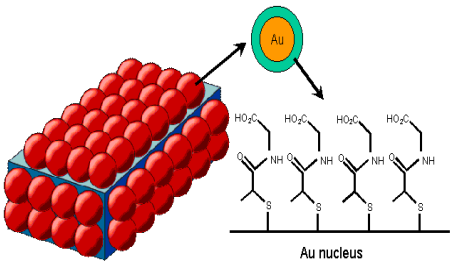
Fig. II.1.2: *AFM images of SiO_2 nanodots on silicon, fabricated through an alumina template.*

d) Self-organized building blocks for nanoelectronic devices.

A. Zoy, V.Ioannou-Sougleridis and A. G. Nassiopoulou

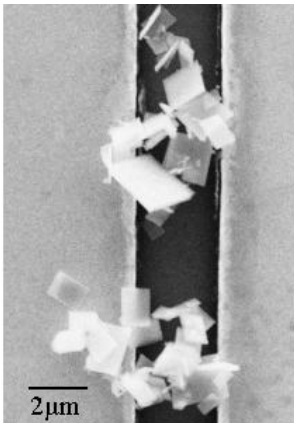
This activity was carried out within the IST ESCHER project (EU Framework program). The main objective was to fabricate self-assembled building blocks for nanoelectronics, using the crystal-lattice-mediated self-assembly process (CLAMS, proprietary process of one of the partners-Strathclyde University). Nanoparticles are self-assembled on microcrystals in a solution by the above technique, which are then self-organized on an oxidized silicon substrate between electrodes by either structural modification of the Si surface between the electrodes or by using field-assisted deposition. The nanoparticles used so far were composed of Au or ZnS and microcrystals were composed of K_2SO_4.

Fig. II.1.3 (a) below shows a block of Au-nanoparticles on K_2SO_4 microcystals. Nanoparticles are composed of a Au nucleus surrounded by tiopronin. *Fig. II.1.3 (b)* shows Au nanoparticle-coated K_2SO_4 microcrystals deposited between Au electrodes by selective field-assisted deposition



(a)

Fig. II.1.3 (a): *Au nanoparticles self-assembled on K_2SO_4 microcrystal. Nanoparticles are composed of a Au nucleus surrounded by tiopronin.*



(b)

Fig. II.1.3 (b): *SEM image of Au nanoparticles-coated K_2SO_4 microcrystals deposited between Au electrodes by electric-field-assisted deposition.*

e) Heat transport simulations in the nanoscale with molecular dymamics.

N. Papanikolaou

Thermal properties on the nanoscale are becoming an important issue as the size of the electronic elements decreases. Our aim is to study the thermal properties of semiconductor materials using molecular dynamics. A classical molecular dynamics simulation program is currently under

development. The program is designed to be general enough to handle different materials as well as to be able to simulate effects like crystallization or growth. We intent to apply molecular dynamics methods to study thermal transport properties in order to elucidate effects like interfacial thermal resistance or modification of the thermal properties in nanostructures like multilayers or dot arrays. The hope is to eventually use computer simulations to design material with tailored thermal properties.

PUBLICATIONS in INTERNATIONAL JOURNALS

1. "Silicon nanocrystals in SiO_2 thin layers", Nassiopoulou A. G., *Encyclopedia of Nanoscience and Nanotechnology*, edited by H. S. Nalwa, vol. 9 p. 793-813 (2004)
2. "Selective self-alignment of Au nanoparticle-coated K_2SO_4 microcrystals in micrometer gratings of V-grooves on a silicon substrate", Nassiopoulou A. G., Zoy A., Ioannou-Sougleridis V., Olzierski A., Travlos A., Martinez-Albertos J. L. and Moore B., *Nanotechnology* 15, 1-5, 352-356, (2004)
3. "Growth of two-dimensional arrays of silicon nanocrystals in thin SiO_2 layers by low pressure chemical vapour deposition and high temperature annealing/oxidation. Investigation of their charging properties", Salonidou A., Nassiopoulou A. G., Travlos A., Ioannou-Sougleridis V. and Tsoi E., *Nanotechnology* 15, 1-7, 1233-1239, (2004)
4. "Transient and ac electrical transport under forward and reverse bias conditions in aluminium/ porous silicon/p-cSi structures", Theodoropoulou M., Karahaliou P. K., Krontiras C. A., Georga S. N., Xanthopoulos N., Tsamis C. and Nassiopoulou A. G., *J. Appl. Phys*. 96, 12, (2004)
5. "Influence of magnetic field on electromagnetic instabilities in Semiconductor superlattices", Tarkhanyan R. H. and Nassiopoulou A. G., *J. Nanosci. Nanotech*. 4, 1085, (2004)
6. "Two-dimensional arrays of nanometer scale holes and nano-V-grooves in oxidized Si wafers for the selective growth of Ge dots or Ge/Si hetero-nanocrystals", Olzierski A., Nassiopoulou A. G., Raptis I. and Stoica T., *Nanotechnology* 15, 1695-1700 (2004)
7. "Transient and ac conductivity of nanocrystalline porous alumina thin films on silicon, with embedded silicon nanocrystals" *J. of Applied Physics*, 95,5, 2776-2780 (2004)

PRESENTATIONS in CONFERENCES

1. "FORUM FIB: Fabrication organization and use of memories obtained by Focused Ion Beam", I. Berbezier, A. Karmous, A. Ronda, T. Stoica, R. Geurt and A.G. Nassiopoulou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004*), November 14-17, Athens, Greece
2. "Ultrafast carrier dynamics in highly implanted and annealed polycrystalline silicon films", E. Lioudakis, A. Othonos and A.G. Nassiopoulou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004*), November 14-17, Athens, Greece
3. "Nanotemplate alumina films on a silicon substrate fabricated by electrochemistry", M.Kokonou, A. G. Nassiopoulou, K. P. Giannakopoulos and N. Boukos, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*, November 14-17, Athens, Greece
4. "Generation of guided terahertz electromagnetic waves in semiconductor superlattices", R.H.Tarkhanyan and A.G. Nassiopoulou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*, November 14-17, Athens, Greece
5. "Investigation of electronic conductivity of nanoparticle coated microcrystals", A. Zoy, A. G. Nassiopoulou, M. Murugesan and B. Moore, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004),* November 14-17, Athens, Greece (to appear in J. of Phys. Conf. Series)
6. "Influence of near interface oxide traps on the charging characteristics of Si nanocrystals embedded within SiO_2", V. Ioannou-Sougleridis and A. G. Nassiopoulou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*, November 14-17, Athens, Greece
7. "Silicon nanocrystal memory cells by low pressure chemical vapor deposition of amorphous silicon on SiO_2 and oxidation", E. Tsoi, P.Normand, A.G. Nassiopoulou, V. Ioannou-Sougleridis and A. Salonidou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*, November 14-17, Athens, Greece
8. "Density of interface traps in ultra thin porous anodic alumina films on silicon", M. Theodoropoulou, P.K. Karahaliou, S.N. Georga, C.A. Krontiras, M.N. Pisanias, M. Kokonou and A.G. Nassiopoulou, *International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004)*, November 14-17, Athens, Greece
9. "Ordered 2-D arrays of Ge quantum dots embedded in ultra thin SiO_2", A. Olzierski, A. G. Nassiopoulou and A. Travlos, *EMRS 2004*, Strasbourg, France
10. "Very thin anodic alumina films with ordered pore arrays on a silicon substrate", M. Kokonou, A. G. Nassiopoulou and K. P. Giannakopoulos, *International Conference on Porous Semiconductor Science and Technology*, Valencia, Spain, March 14-19, 2004
11. "Photoluminescence of very thin anodic alumina films on a silicon substrate", M. Kokonou and A. G. Nassiopoulou, *International Conference on Porous Semiconductor Science and Technology*, Valencia, Spain, March 14-19, 2004
12. "2-D arrays of Ge quantum dots in SiO_2 for non-volatile memories", A. Olzierski, A. Nassiopoulou, A. Travlos, T. Stoica, *XX Panhellinion Conference on Solid State Physics and Materials Science26-29 September*, Ioannina 2004
13. "Porous alumina thin films on Si with self-assembled vertical pores", M. Kokonou, A. G. Nassiopoulou and K. P. Giannakopoulos, *XX Panhellinion Conference on Solid State Physics and Materials Science26-29 September*, Ioannina 2004
14. "Study of interface state density in porous alumina/c-Si MOS structures", M. Theodoropoulou, P. Karachaliou, S. N. Georga, C. Krontiras, M. Pizanias, M. Kokonou and A. G. Nassiopoulou, *XX Panhellinion Conference on Solid State Physics and Materials Science26-29 September*, Ioannina 2004

INVITED TALKS

1. "Low dimensional Si or Ge for application in nanodevices", A. G. Nassiopoulou, **Invited talk**, *International Workshop on ultimate Lithography and Nanodevice Engineering*, Agelonde, France, 13-16 June 2004
2. "2-D arrays of Semiconductor nanocrystals in thin SiO_2 layers application in quantum dot memories", A. G. Nassiopoulou, **Invited talk**, *E-MRS spring Meeting Symposium I*, May 24-28, 2004
3. "Low-dimensional Si for optoelectronics and memory devices, A. G. Nassiopoulou, **Invited talk**, *NATO Advanced Study Institute on Nanostructured and Advanced Materials for Optoelectronic, Photovoltaic & Sensor applications*, Sozopol, Bulgaria, September 6-17, 2004