Project II. 2: SILICON NANOCRYSTAL MEMORIES

Project leader: P. Normand

Other key researchers (From the Institute): C. Tsamis

Post-doctoral: D. Skarlatos, V. Vamvakas

PhD candidates: E. Kapetanakis, P. Dimitrakis, S. Koliopoulou

External collaborators: D. Tsoukalas (NTUA)

Projects Running:

- EC GROWTH GRD1-2000 -Nanocrystals for electronic applications, NEON- N°25619

Goals :

- To explore and develop novel technological routes for generating nanocrystal based structures aiming at electronic memory applications.

- To fabricate, evaluate and optimize nanocrystal memory devices for low-voltage high-density data storage.

- To transfer laboratory nanocrystal memory technology to industry.

Main results:

a) Silicon nanocrystal memory devices obtained by low-energy ion-beam-synthesis

Nonvolatile memory technology using discrete charge storage nodes embedded in the gate oxide of metal-oxide-semiconductor (MOS) devices offers an attractive alternative for extending the scaling of conventional floating-gate memories. Among the various processing routes explored during the last few years for generating such storage nodes in the form of nanocrystals (NCs), the ion-beam-synthesis (IBS) technique has received substantial attention due to its flexibility and manufacturing advantages. The potential of IBS for NC-based memories operating at low voltages has been recently enhanced through the synthesis in the low-energy (LE) regime (typically 1keV) of single Si-NC layers in thin SiO_2 films. Thanks to NEON European framework, the LE-IBS technique surpassed the level of 'proof of concept' and promising devices for true nonvolatile memory applications have been recently achieved at IMEL (Dimitrakis et al. SSE 2004). In addition to the numerous materials and electrical studies developed for understanding and manipulating the formation of Si NCs by LE-IBS (Bonafos et al. JAP 2004), major efforts have been devoted to identify and solve fabrication issues encountered during the integration of this technique in a manufacturing environment (Normand et al. NIMB 2004).

Prototype nanocrystal memory devices were recently fabricated at STMicroelectronics on 8-inch wafers using a conventional process flow based on a 0.15μm Flash-EEPROM technology. The devices were isolated following a shallow-trench-isolation (STI) procedure. N-MOSFETs memory cells with gate lengths and widths ranging from 0.16 to 10 μm have been achieved. Taking into account electrical investigations conducted at STM and IMEL, it was concluded that these devices suffer from high boron contamination that leads to large threshold voltage shifts and variations across the wafers. Despite this cross-contamination effect that occurs during Si implantation, small fluctuations in memory windows under P/E operation were observed in the case of large-channel transistors. This result is important since it suggests that the LE-IBS process was quite uniform over the wafers.

Most important of all, our investigations showed that parasitic transistors (FET_P) affect drastically the device performance. The action of FET_P that can be detected through a "subthreshold hump" in the transfer characteristics of the MOSFETs leads to a substantial degradation of the electrical properties of the intended devices and dominates the memory behavior of deep submicronic cells. This detrimental effect goes maybe beyond the LE-IBS-related-concerns and could constitute a technological issue towards the integration of NC floating-gate in conventional memory architecture (see Dimitrakis and Normand MRS Fall Meeting 2004).

b) Memory devices obtained by Si^+ irradiation through poly-Si/SiO_2 gate stack

As already emphasized the LE-IBS technique leads to promising device results and many fabrication issues have been identified and solved for its integration at an industrial level. However, while ion implantation into uncapped gate oxides offers a number of processing alternatives for damage recovery, removal of near surface atoms (sputtering effect) during implantation and oxide contamination (e.g. from ambient moisture) between the implantation and annealing steps cannot be avoided. To be efficient, the alternative of using a protecting layer (e.g. poly-silicon) deposited onto the

gate oxide before ion implantation would require high-energy implants and thus, the advantages of the LE-IBS technique will be rapidly lost.

In an effort to overcome this concern, NEON Partners from Research Center Rossendorf have recently proposed a different approach using Si ion irradiation through a poly-Si/SiO_2 gate stack. Fabrication of memory devices exploiting the above technique has been successfully achieved at ZMD (Zentrum Mikroelektronik Dresden AG) on 6 inch wafers using 0.6 μm CMOS technology rules. These devices were tested by ZMD and IMEL. The charge storage characteristics of these devices for different process conditions (Si irradiation fluence, thermal budget) have been examined in terms of memory windows for different programming/erasing times and voltages. Endurance to successive program/erase cycles and retention time characteristics up to 125°C of selected devices have been also tested. Low-voltage and high-speed operating memory cells that can endure 10^7 programming/erasing cycles have been demonstrated. While excellent device uniformity and reproducibility have been observed over the wafers, data retention evaluation reveals that more research is still required to fine tune the fabrication process and insure a 10-year memory window for nonvolatile memory applications (see Dimitrakis et al. MMN 2004 Conference).

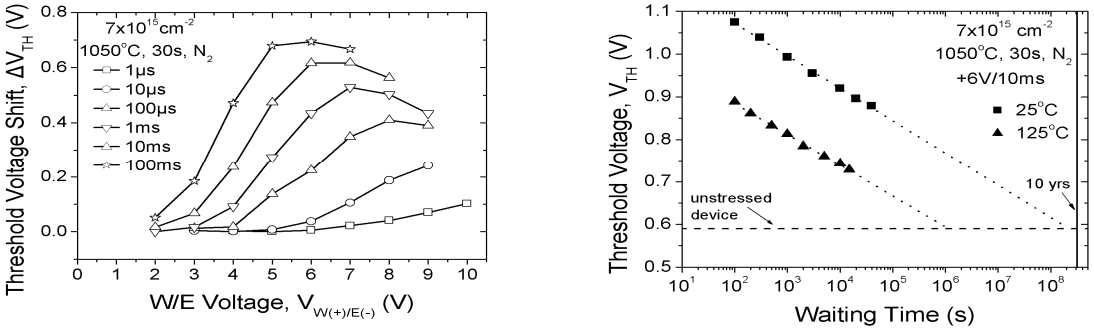

Fig. II.2.2: *Single-MOSFET memory cell obtained by Si ion irradiation through the poly-Si/SiO_2 gate stack.* ***Left:*** *Memory windows obtained by sequential W/E pulses with different heights and widths.* ***Right:*** *Charge retention characteristics at room temperature (RT) and 125 °C.*

c) Ge nanocrystals in MOS-memory structures produced by molecular-beam epitaxy and rapid-thermal processing

Our team was here in charge of the electrical characterization of SiO_2 layers with embedded Ge nanocrystals obtained by a molecular beam epitaxy (MBE) based process developed at the University of Aarhus (DK) within NEON framework. This process allows the generation of a sheet of crystalline Ge nanodots at any wanted depth in the oxide. Production of an area-dot density of $5x10^{11}$ cm^{-2} of crystalline Ge dots of 4 nm in diameter located in the silicon oxide at 3-4 nm from the Si/SiO_2 interface has been demonstrated. Charge storage behavior of these structures has been investigated through C-V and I-V measurements of Al gate capacitors (*see Kanjilal et al., Appl. Phys. A 2004*). Memory windows of about 0.2 and 0.5 V for gate voltage round sweeps of 3 and 6 V, respectively, corresponding to electric fields around 2.22 and 4.44 MV/cm have been achieved. The density of interface states at mid-gap evaluated through quasistatic and high-frequency C-V measurements is on the order of 10^{11} $eV^{-1}cm^{-2}$. Although further investigations in terms of charge retention time and write/erase pulsed operation are required to definitively conclude on the memory behaviour of oxides with embedded MBE-formed Ge nanocrystals, the above results indicate that the MBE method is well-suited for the further development of nanocrystal floating gate memory cells.

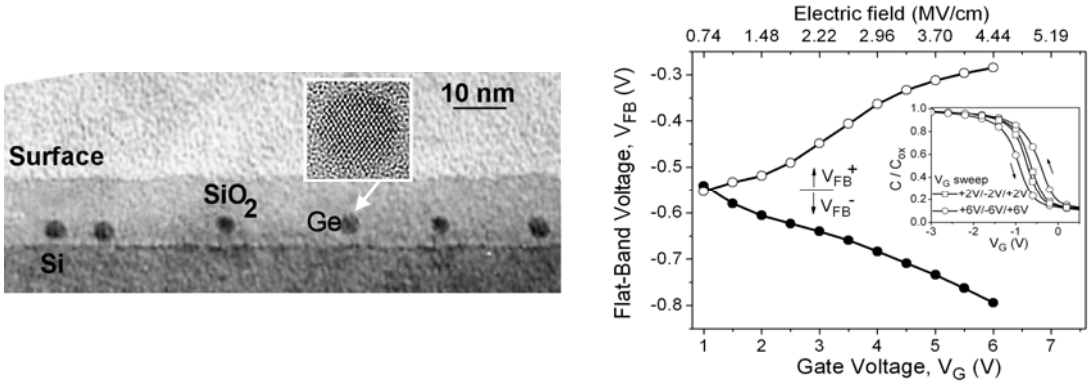

Fig. II.2.3: Left: *Bright field TEM image of a cross-section sample with a 0.7 nm thick Ge layer after oxidation at 800°C for 14 min followed by reduction at 950 °C for 30 in N_2. Insert: high-resolution TEM picture of a Ge nanocrystal.* ***Right:*** *Flat-band voltage vs gate voltage (V_G) characteristics for different $+V_G/-V_G/+V_G$ sweep sequences of a 14nm-thick oxide layer with embedded Ge nanocrystals.*

d) Hybrid silicon-organic memory devices using gold nanoparticles

This research aims at the exploration of an inexpensive technology that combines silicon nanofabrication techniques and the emerging area of intra-molecular electronics to develop high-density memory arrays. This activity is conducted in close collaboration with the University of Durham and was initiated within the framework of the IST-FET European project Fracture (2001-2003). Last year, our research activities have been concentrated on the fabrication of hybrid memory nanoparticle FET devices using conventional silicon process steps integrated with chemical processing for nanoparticle deposition and Langmuir-Blodget deposition technique for organic insulator deposition (control insulator). These films were deposited on top of a thermal oxide that makes the interface with the silicon channel (tunnelling oxide). The devices exhibit non-volatile memory characteristics and remain stable at room temperature for an investigated retention time of 6 months.

This year, we demonstrated MISFET memory devices that incorporate a monolayer of Langmuir-Blodgett (LB)-deposited-gold nanoparticles as floating-gate charge storage elements (Kolliopoulou et al. MRS Fall Meeting 2004). The devices were fabricated on a SOI substrate using conventional silicon processing. The nanoparticle layer was separated from the channel area of the FET with a 5 nm thermal SiO_2 layer and isolated from Al gate contact with a LB-deposited organic (Cadmium Arachidate, CA) insulator layer. The memory behavior of the devices was evaluated under pulsed gate-voltage operation conditions. While significant nanocrystal charging from the channel is detected at low voltage pulses (< 5 V), charge injection from the gate occurs for higher voltages due to the poor insulating properties of the CA layer. Replacement of the later with a less conductive material is underway for device performance improvement.

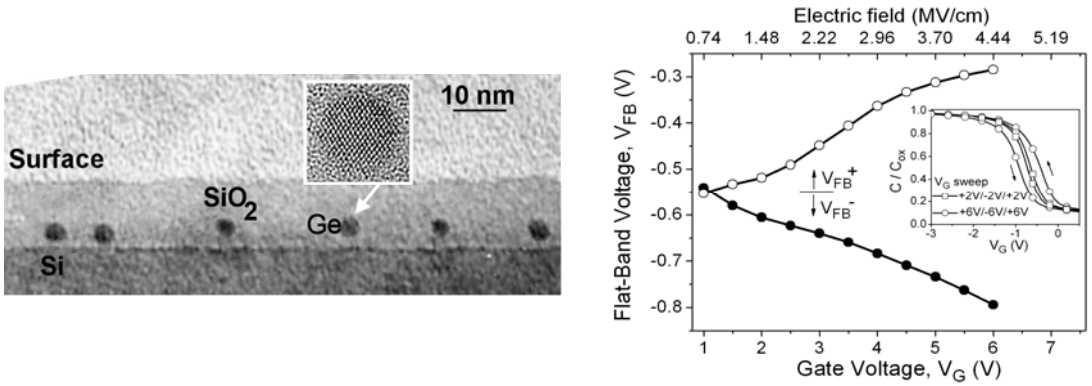

Fig. II.2.3: Left: *Bright field TEM image of a cross-section sample with a 0.7 nm thick Ge layer after oxidation at 800°C for 14 min followed by reduction at 950 °C for 30 in N_2. Insert: high-resolution TEM picture of a Ge nanocrystal.* ***Right:*** *Flat-band voltage vs gate voltage (V_G) characteristics for different $+V_G/-V_G/+V_G$ sweep sequences of a 14nm-thick oxide layer with embedded Ge nanocrystals.*

PUBLICATIONS in INTERNATIONAL JOURNALS

1. "Nanocrystals manufacturing by ultra-low-energy ion-beam-synthesis for nonvolatile memory applications", P. Normand, E. Kapetanakis, P. Dimitrakis, D. Skarlatos, K. Beltsios, D. Tsoukalas, C. Bonafos, G. Ben Asssayag, N. Cherkashin, A. Claverie, J. A. Van Den Berg, V. Soncini, A. Agarwal, M. Ameen, M. Perego, M. Fanciulli, *Nucl. Instr. Meth. Phys. Res. B (NIMB*) 216, 228-238 (2004)
2. "Silicon nanocrystal memory devices obtained by ultra-low-energy ion-beam-synthesis", P. Dimitrakis, E. Kapetanakis, D. Tsoukalas, D. Skarlatos, C. Bonafos, G. Ben Asssayag, A. Claverie, M. Perego, M. Fanciulli, V. Soncini, R. Sotgiu, A. Agarwal, M. Ameen, P. Normand, *Solid State Electronics* 48, 1511-1517 (2004)
3. "Manipulation of two-dimensional arrays of Si nanocrystals embedded in thin SiO_2 layers by low energy ion implantation", C. Bonafos, M. Carrada, N. Cherkashin, H. Coffin, D. Chassaing, G. Ben Assayag, A. Claverie, T. Muller and K. H. Heinig, M. Perego and M. Fanciulli, P. Dimitrakis, P. Normand, *J. Appl. Phys*. 95, 5696-5702 (2004)
4. "Size and aerial density distributions of Ge nanocrystals in a SiO_2 layer produced by molecular beam epitaxy and rapid thermal processing", A. Kanjilal, J. Lundsgaard Hansen, P. Gaiduk, A. Nylandsted Larsen, P. Normand, P. Dimitrakis, D. Tsoukalas, N. Cherkashin, A. Claverie, A*ppl. Phys. A - Mater. Sc. Process. Online* (June 2004)
5. "Processing issues in silicon nanocrystal manufacturing by ultra-low-energy ion-beam-synthesis for non-volatile memory applications", P. Normand, P. Dimitrakis, E. Kapetanakis, D. Skarlatos, K. Beltsios, D. Tsoukalas, C. Bonafos, H. Coffin, G. Benassayag, A. Claverie, V. Soncini, A. Agarwal, Ch. Sohl, M. Ameen, *Microelectronic Engineering* 73-74, 730-735 (2004)
6. "Integration of organic insulator and self-assembled gold nanoparticles on Si MOSFET for non-volatile memory cells", S. Kolliopoulou, P. Dimitrakis, P. Normand, H-L. Zhang, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, D. Tsoukalas, Microelectronic Engineering 73-74, 725-729 (2004)

PRESENTATION IN CONFERENCES

1. "Memory devices obtained by Si^+ irradiation through poly-Si/SiO_2 gate stack", P. Dimitrakis, P. Normand, E. Votintseva, K-H. Stegemann, K-H. Heinig, B. Schmidt, **Oral presentation**, *International Conference on Microelectronics Microsystems Nanotechnology, MMN 2004*, Athens, Greece, November 14-17 (2004)
2. "Field effect devices with metal nanoparticles integrated by Langmuir-Blodgett technique for non-volatile memory applications", S. Kolliopoulou, D. Tsoukalas, P.Dimitrakis, P. Normand, S. Paul, C. Pearson, A. Molloy, M. C. Petty, **Poster presentation**, *International Conference on Microelectronics Microsystems Nanotechnology, MMN04*, Athens, Greece, November 14-17 (2004)

INTERNATIONAL CONFERENCE PROCEEDINGS

1. "Manipulation of 2D-Arrays of Si Nanocrystals Embedded in a Thin SiO_2 Layer by Low Energy Implantation", C. Bonafos, G. Ben Assayag, S. Schamm, H. Coffin, N. Cherkashin, A. Claverie, P. Normand, P. Dimitrakis, M. Perego, M. Fanciulli, T. Mueller, K-H. Heinig, M. Tence, C. Colliex, **Oral presentation**, *Materials Research Society Fall Meeting 2004, MRS Fall 04*, Symposium D, Boston, USA, November 29 - December 3 (2004)
2. "Ge Nanocrystals in MOS-Memory Structures Produced by Molecular-Beam Epitaxy and Rapid-Thermal Processing", A. Nylandsted Larsen, A. Kanjilal, J. L. Hansen, P. Gaiduk, P. Normand, P. Dimitrakis, D. Tsoukalas, N. Cherkashin, A. Claverie, **Poster presentation**, *Materials Research Society Fall Meeting 2004, MRS Fall 04, Symposium D*, Boston, USA, November 29 - December 3 (2004)
3. "Oxidation of Si nanocrystals obtained by low energy ion implantation in a thin SiO_2 layer", H. Coffin, C. Bonafos, N. Cherkashin, S. Schamm, G. Ben Assayag, G. Zanchi, P. Dimitrakis, P. Normand, M. Tence, C. Colliex, A. Claverie, **Poster presentation**, *Materials Research Society Fall Meeting 2004, MRS Fall 04, Symposium D*, Boston, USA, November 29 - December 3 (2004)
4. "Gold Langmuir-Blodgett deposited nanoparticles for non-volatile memories", P. Dimitrakis, S. Kolliopoulou, D. Tsoukalas, P. Normand, S. Paul, C. Pearson, A. Molloy, M. C. Petty, **Poster presentation**, *Materials Research Society Fall Meeting 2004, MRS Fall 04, Symposium D*, Boston, USA, November 29 - December 3 (2004)
5. "A Si/SiGe MOSFET utilizing low-temperature wafer bonding", S. Kolliopoulou, P. Dimitrakis, D. Goustouridis, S. Chatzandroulis, P. Normand, D. Tsoukalas, H. Radamson, **Poster presentation**, *International Conference on Micro-and Nano-Engineering, MNE04*, Rotterdam, Netherlands, September 19-22 (2004)
6. "Single electron charging mechanisms into silicon quantum dots realized by ultra low energy implantation", **Oral presentation**, A. Beaumont, P. Normand, G. Ben Assayag, A. Claverie, A. Souifi, *European Materials Research Society Conference, E-MRS04*, Strasbourg, France, June (2004)

INVITED TALKS

1. "Semiconductor nanocrystal floating-gate memory devices", P. Dimitrakis and P. Normand, **Invited talk**, *Materials Research Society Fall Meeting 2004, MRS Fall 04, Symposium D*, Boston, USA, November 29 - December 3 (2004)
2. "Nanocrystal memory for future electronics", P. Normand, **Invited talk**, *13th European Workshop on Heterostructure Technology, HETECH 2004*, Heraklion, Greece, October 3-6 (2004)