Project III. 1: POROUS SILICON TECHNOLOGY and APPLICATIONS

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Funding:

- EU Marie Curie/ ''RF on porous'', re-integration grant, Contract N^0 016142, 29/7/2005-28/7/2007
- Contract from the National Research Agency-Cyprus, Photothermal analysis, 1/7/2004-30/6/2006
- Contract with the company Unilever UK, Flow system for Unilever, 1/12/2005-31/5/2007
- Contract with the company ST Microelectronics SA France, RF-on-porous, 30/7/2005-30/7/2008

Research orientation:

- Material development (Nanoporous or macroporous silicon)
- Development of micromachining processes
- Application in flow sensors, accelerometers, microfluidic devices and on-chip integration of RF components.

a) Porous silicon technology for sensors

A big effort has been devoted the last years at IMEL in developing enabling processing technologies and materials for different applications including sensors and systems. One such technology with important potential for applications is porous silicon technology.
Porous silicon is a nanostructured material which may be formed locally on a silicon substrate by electrochemistry. It presents high thermal and electrical resistivity and it may be used as a micro-hotplate material in silicon thermal sensors. In addition, porous silicon shows etching selectivity compared to bulk silicon and it is a very good sacrificial material for bulk silicon micro-machining.
Important expertise and know how on porous silicon have been developed at IMEL within different EU and national projects, as well as within direct contracts with industry, including:

- Proprietary micromachining techniques based on the use of porous silicon as a sacrificial layer for the fabrication of free standing silicon membranes, bridges and cantilevers on silicon
- Technologies using porous silicon for local thermal isolation on a silicon wafer, for RF isolation or as a matrix for the deposition of catalytic materials for chemical sensors

b) RF integration on porous silicon

This activity started at IMEL in 2004 with the overall objective:

- to explore and extend porous silicon technology into the domain of CMOS-compatible integrated RF systems for use in systems-on-chip and
- to improve the performance of currently integrated analog CMOS components by above technology transfer and related optimization of design methodologies.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Macroporous silicon

D. N. Pagonis, F. Zacharatos and A. G. Nassiopoulou

A process for the formation of both ordered and non-ordered macroporous silicon has been developed (fig. III.1.1a & III.1.1b). The resulting structure consists of an array of vertical pores perpendicular to the silicon substrate. The diameter of the developed pores is in the range of 1 to 10 micrometers depending on the type (non-ordered or ordered) of the macroporous silicon formed. The thickness of the macroporous layer can exceed 100 μm. On-going research involves the development of appropriate masking techniques for the confined formation of both types of macroporous silicon locally on a particular area of the silicon substrate.

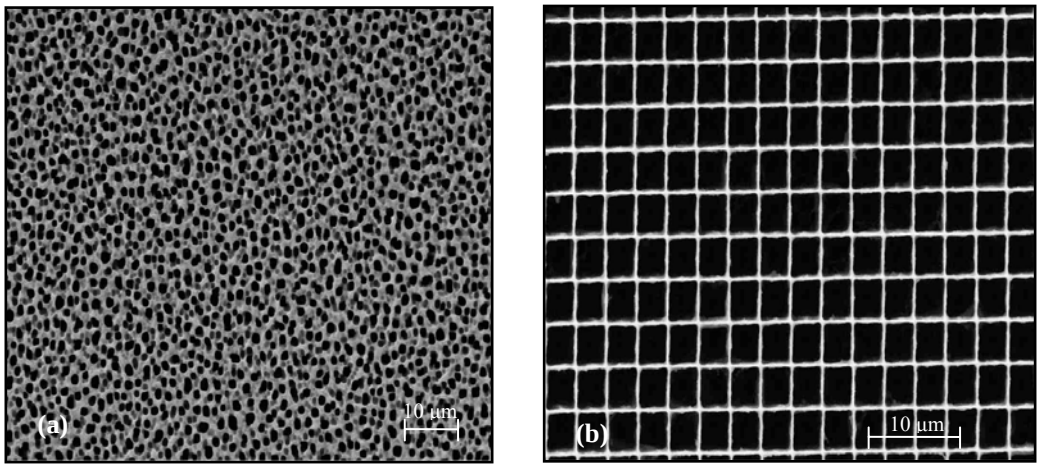

Fig. III.1.1: *SEM image of a typical non-ordered macroPS layer formed on a p-type silicon substrate. In* ***(a)*** *we see a top view, while in* ***(b)*** *a cross-sectional view of the structure. The thickness of the layer is about 9.5 μm.*

A technique for the formation of double porous silicon layers of different pore morphology has also been developed. The resulting structure consists of a layer of macroporous silicon situated above a nanoporous silicon one (fig. III.1.2a). The pore diameter of the layer underneath is in the nanometer scale. Furthermore, by proper selective wet-etching, the nanoporous silicon can be removed, resulting in a free-standing macroporous silicon membrane (fig. III.1.2b). The depth of the cavity situated underneath the membrane is directly proportional to the thickness of the nanoporous silicon layer, formed at a previous stage of the process.

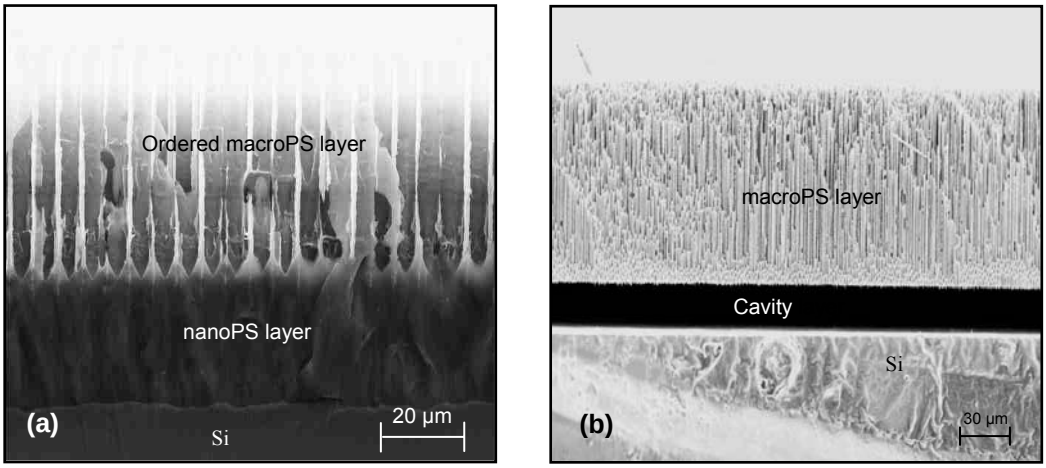

Fig. III.1.2: *Cross-sectional SEM images of typical structures consisting of macroporous silicon over nanoporous silicon before* ***(a)*** *and after* ***(b)*** *the selective etch of the nanoporous layer.*

Task 2 Flow sensor with microfluidic channel

D. N. Pagonis, A. Petropoulos, G. Kaltsas and A. G. Nassiopoulou

This work concerns the fabrication, modeling and characterization of a novel microfluidic flow sensor using porous silicon technology for the fabrication of the microfluidic channel (fig. III.1.3). The novel microfluidic flow sensor is compatible with Si technology, thus allowing for integration on the same chip of the appropriate read-out electronics. The microchannel is sealed by a porous silicon membrane, thus the final structure is co-planar with the rest of the substrate.The fabrication technology of buried microchannels in silicon using porous silicon technology has been developed in a previous work; the technique is based on two consecutive steps of anodization and electropolishing of p-type silicon.The sensor's basic components are the buried microchannel, a central heater and appropriate temperature sensing elements, all integrated on top of the channel.

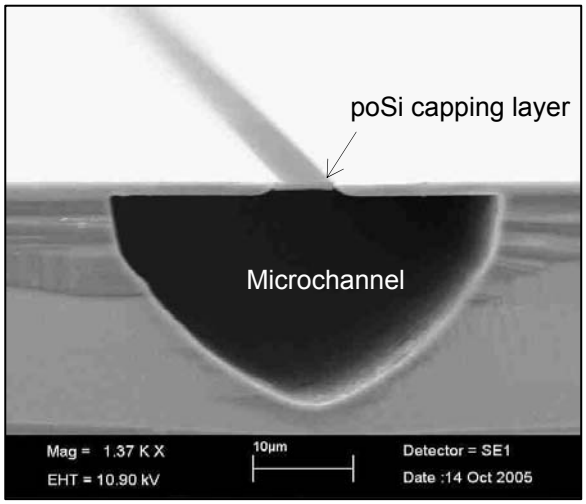

Fig. III.1.3: *SEM picture of the cross-section of the microchannel of the microfluidic sensor. The thickness of the capping nano-porous silicon layer is about 1 μm, while the depth of the cavity underneath is about 20 μm.*

The principle of operation of the device can be simply described as follows: assuming there is no liquid flow inside the microchannel, a symmetric thermal distribution is developed on top of the capping layer in the immediate vicinity of the heater. When flow is present, appropriate resistors which are integrated at both sides of the heater detect the asymmetry of the thermal distribution, induced from the flow of the liquid in the channel. The inlet and outlet of the device are situated at the two ends of the buried channel. A typical simulation result of the developed liquid flow inside the microchannel is shown in fig. III.1.4; general characteristics of the flow can be derived from modeling results. Current on-going research includes the characterization of the device.

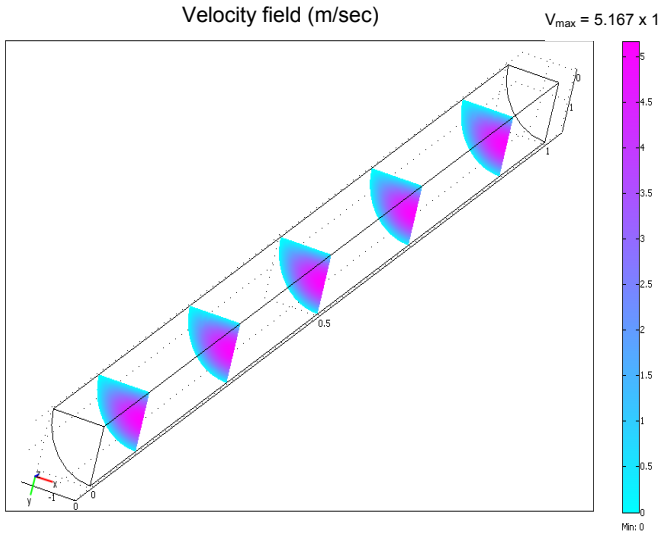

Fig. III.1.4: *Simulation results for a developed water flow inside the microchannel of the sensor. The value of the inlet velocity is 26.5 μm/sec, corresponding to a liquid flow of 1 nanoliter / min.*

Task 3 Integrated inductors on Porous Silicon in CMOS-compatible processes

H. Contopanagos, D. Pagonis and A. G. Nassiopoulou

Radio-frequency (RF) components such as inductors, capacitors, transformers and other resonators, integrated on-chip, are essential building blocks of all analog radio frequency integrated circuits (RFICs) and their performance at current and future CMOS processes is a major bottleneck to successful system integration. It is clear that fully on-chip inductors in a CMOS-compatible process substantially improving the current art could create an important competitive advantage in the overall performance/cost ratio compared to hybrid technologies. In this work we propose the use of porous silicon as a compact micro-plate with low RF losses, grown locally on the silicon substrate by electrochemistry, as a way to implement significantly higher-Q RF inductors on a standard CMOS technology. We have first assessed the use of porous silicon isolation technology in combination with a standard CMOS technology by a) developing simulation-based inductor designs on 0.18μm CMOS technology and validating these simulations by comparison to measurements (fig. III.1.5) and then by b) extracting through simulation the inductor characteristics (same layout) when the silicon substrate is replaced by a porous silicon layer of a given thickness, dielectric constant and loss tangent (fig. III.1.6a). We find Q-factor enhancements of 50% or more in that technology.

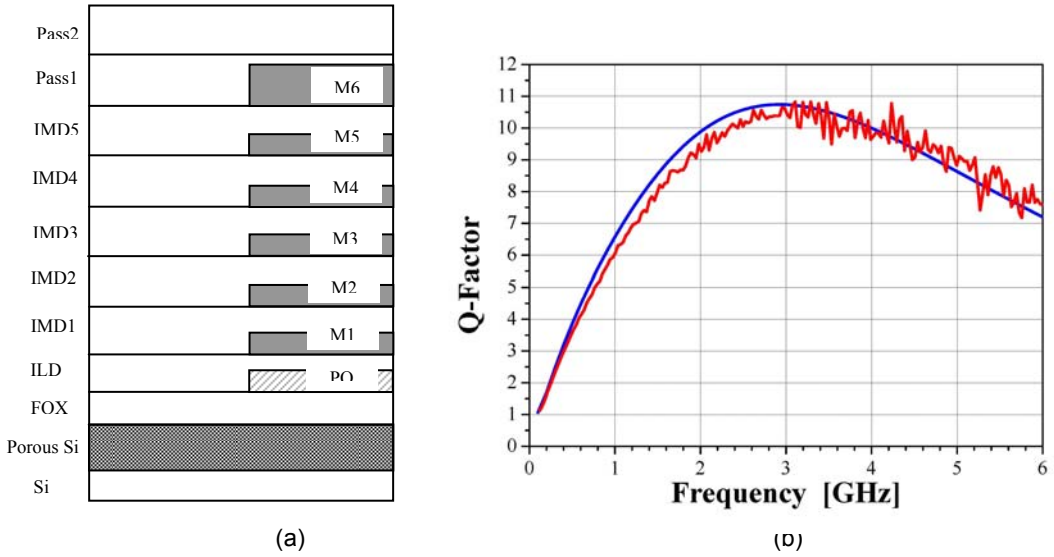

Fig. III.1.5: a) *Typical 0.18μm 6-metal CMOS interconnect diagram and Porous Si layer,* ***b)*** *Q-factor of a 5-metal-layer inductor on 0.18μm CMOS without Porous Si: Blue=Theoretical, Red=Measurements.*

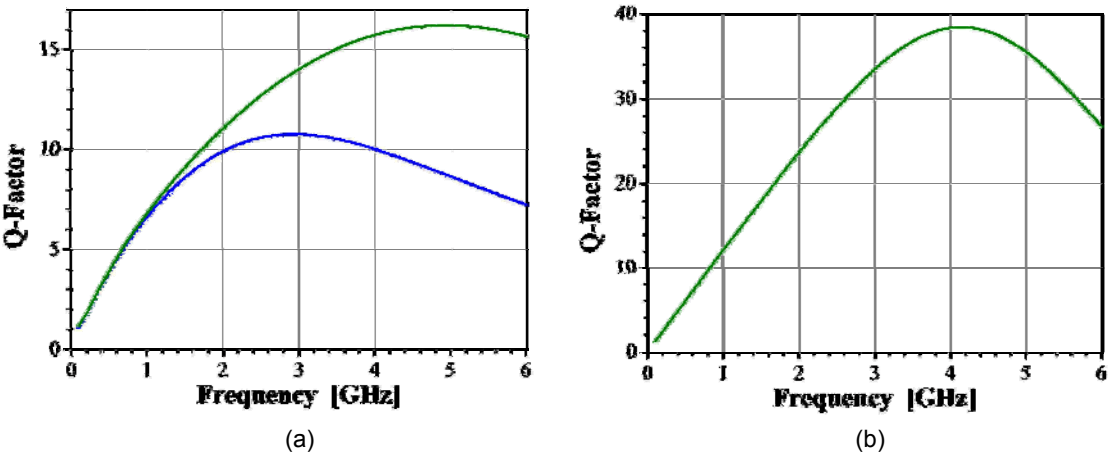

Fig. III.1.6: a) *Simulated Q-factor of the inductor of fig.III.1.5 without Porous Si (Blue) and with porous Si (Green).* ***b)*** *Simulated performance of an optimized 2-metal Cu inductor compatible with CMOS 0.13μm technology.*

PROJECT OUTPUT in 2005

PUBLICATIONS in REFEREED JOURNALS

1. “Electronic structure of C60, CuPc and C60/CuPc nanoparticles and their layers”, I. Lysko, A. Gorchinskiy, E. Buzaneva, C. Tsamis, A. G. Nassiopoulou, P. Scharff, L. Carta-Abelmann, K. Risch, Fullerenes, Nanotubes and Carbon Nanostructures 13(3), 259 (2005)
2. "Porous Si for sensor applications", A. G. Nassiopoulou (invited paper) in "Nanostructured and Advanced Materials", edited by: A. Vaseashta, D. Dimova-Malinovska and J. M. Marshal, NATO Science Series II. Mathematics, Physics and Chemistry, vol. 204, pages 189-204, (2005)
3. “Investigations by X-ray topography of quartz and lengasite resonators”, I. Mateescu, B. Capelle, J. Detaint, G. Johnson, E. Tsoi, C. Bran, J. Phys. IV France 126 (2005) 3-6

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Generation of guided terahertz electromagnetic waves in semiconductor superlattices”, R. H. Tarkhanyan and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 19-22 (2005)
2. “Combination of integrated thermal flow and capacitive pressure sensors for high sensitivity flow measurements in both laminar and turbulent regions”, G. Kaltsas, D. Goustouridis, A. G. Nassiopoulou and D. Tsoukalas, J. Phys.: Conf. Ser. 10 277-280 (2005)
3. “A microcontroller-based interface circuit for data acquisition and control of a micromechanical thermal flow sensor”, P. Asimakopoulos, G. Kaltsas and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 301-304 (2005)
4. “Stress characteristics of suspended porous silicon microstructures on silicon”, K. Anestou, D. Papadimitriou, C. Tsamis and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 309-312 (2005)
5. “Metamorphic Electromagnetic Media”, C. Kyriazidou, H. Contopanagos and N. Alexopoulos, Proceedings of the 9th Intern. Conf. On Electromagnetics in Adv. Applications ICEAA 2005 (September 2005), Torino, Italy, pp. 965-968.
6. “Electromagnetic design methods in systems-on-chip: Integrated filters for wireless CMOS RFICs”, H.Contopanagos, Journal of Physics, Conference Series, Vol.10, 2005, pp. 337-342.

INVITED TALKS

1. “More than Moore: Technologies for Nanoelectronics, MEMs and other emerging applications”, Androula G. Nassiopoulou, ISNM 2005 (Third International Symposium on Nanomanufacturing), Limassol. Cyprus, November 3-5, 2005
2. “Embedded Antennas and Matching Networks in wireless communications”, H. Contopanagos, WSEAS International Conference on Engineering Education, July 8-10 2005, Athens, Greece.

CONFERENCE PRESENTATIONS

1. “Study of a Novel Thermal Accelerometer System”, G. Kaltsas, D. Goustouridis and A. G. Nassiopoulou, Eurosensors XIX, Barcelona, Spain, Sept. 11-14, 2005.
2. “Macroporous silicon with regular arrays of vertical pores on p-type wafers”, D. N. Pagonis, J. Semai and A. G. Nassiopoulou, XXI Panhellenian Conference on Solid State physics and Materials Science, Nicosia, Cyprus 28-31 August 2005
3. "Technology for the formation of Macroporous silicon over Cavity", D.N. Pagonis, J. Semai and A.G. Nassiopoulou, International Conference on Micro and Nano Engineering, Vienna, Austria19-22 Sept., 2005
4. "Free-Standing Macroporous Silicon Membranes Over Nanoporous/Cavity by Electrochemical Process" , D. N. Pagonis, J. Semai and A. G. Nassiopoulou, 3rd International Symposium on Nanomanufacturing (ISNM 2005), Nicosia, Cyprus, November 3-5, 2005
5. “Metamorphic Electromagnetic Media”, 9th International Conference On Electromagnetics in Advanced Applications ICEAA 2005, September 12-16 2005, Torino, Italy.

EDITION of CONFERENCE PROCEEDINGS

1. Edition of the Proceedings of the International conference of PSST on Porous Semicondictor Science and Technology, held in Cullera-Valencia, 14-19 March 2004, Special Issue of Physica Status Solidi, Guest editors: L. Canham, A. G. Nasiopoulou, and V. Partkhutic, Wiley-VCH, (2005)
2. Proceedings of the Second International Conference on Microelectronics, Microsystems and Nanoelectronics (MMN), held at NCSR Demokritos in Athens on 14-17 November 2004. Special issue of the Institute of Physics: Conf. Series (Editors: A. G. Nassiopoulou, N. Papanicolaou, C. Tsamis). Published also on-line at jpconf.iop.org (2005)