Project III. 4: THIN FILM DEVICES FOR LARGE AREA ELECTRONICS

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Funding:

- GSRT – PENED, Development of polysilicon TFT technology with advanced techniques of film annealing and device characterization, 15/12/2005 – 14/12/2008
- GSRT-Bilateral project Greece-Serbia, Performance, stress degradation and reliability characterization of thin film transistors for the investigation of defects in polycrystalline silicon films, 5/11/2004-5/11/2006

Research orientation:

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors fabricated in such films. Specifically, the targets are:

- Evaluation of device parameter (a) hot carrier and (b) irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films.
- Investigation of effects of variations in TFT structure and fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Investigation of the influence of film thickness and crystallization technique on defects and on device degradation for ELA technology optimization.
- Evaluation of bias stress-induced instabilities in solid phase crystallized (SPC) TFTs.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Characterization and hot carrier stress investigation

The characterization of TFTs made in sequentially laterally solidified (SLS) ELA polysilicon films has yielded systematic trends, with respect to the film thickness, in the device parameter values. For TFTs in "directional" SLS ELA films, which have very elongated grains along a preferred direction, the extracted average device parameters, as a function of the active layer thickness, are summarized in the following table:

Polysilicon Thickness (nm)	Field Effect Mobility, μ (cm²/Vs)	Threshold Voltage, V_{th} (V)	Subthreshold Slope, ***s*** (V/dec)	Domain Boundary Trap Density, N_t (cm^{-2})
30	160	-4.1	0.13	6.7×10^{11}
50	430	-1.1	0.11	4.9×10^{11}
100	580	-1.3	0.13	4.0×10^{11}

Clearly, the electron mobility increases and the estimated trap density decreases, indicating better material quality, with increasing film thickness. Furthermore, hot electron stressing measurements, to investigate trap generation and device parameter degradation, have been expanded to the case of TFTs fabricated in 50 nm thick 2^N-shot polysilicon films. This is an advanced variation of the SLS ELA technique that utilizes laser exposure through masks with many parallel slits and affords much better "grain engineering", that is, good control of grain shapes, as well as better intragrain material quality. TFTs are subjected to DC gate and drain bias hot electron stresses under worst ageing conditions (V_{GS} = $V_{DS}/2$). In fig. III.4.1, the threshold voltage and subthreshold swing shifts ΔV_{th} and Δs, as well as the degradation of the transconductance G_m, are shown against the stressing time, for a stressing condition of (V_{GS}, V_{DS}) = (5 V, 10 V).

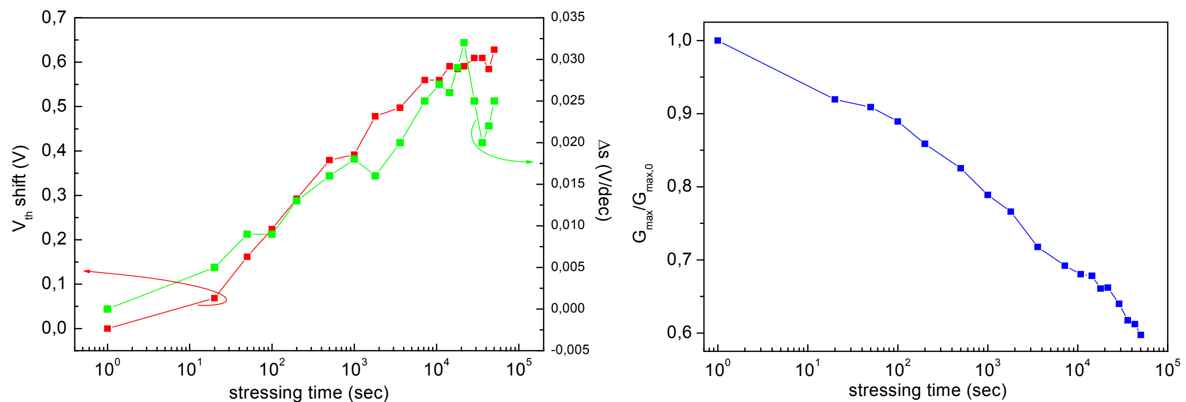


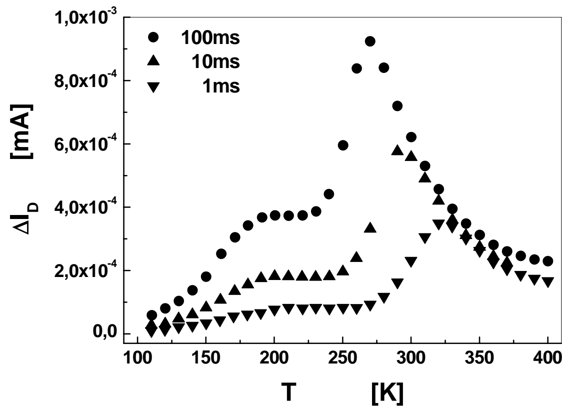
Fig. III.4.1: *V_{th} and s shifts (left) and G_m degradation (right) with stressing time for TFTs with (W, L) = (8 μm, 1.5 μm) in 2^6-shot SLS ELA polysilicon films.*

The V_{th}, *s* and g_m degradations are observed to be approximately logarithmic with stress time, indicating some active layer and interface degradation due to trap creation. The degree of degradation is similar to that earlier obtained for TFTs in directional polysilicon of the same thickness. The trap generation in the active layer is quantified, with respect to the trap density in unstressed material, by utilizing the *s* degradation.

Task 2 Transient current analysis

The drain current transients obtained in directional or 2^N-shot type SLS ELA TFTs are of the same order of magnitude at dark as well as under illumination, indicating material of high crystalline quality with low defect density. Moreover, the DLTS signals $\Delta I_{DS}/I_{DS}$ fall sharply at cryogenic temperatures, indicating a carrier generation freezeout. From these characteristics, a low concentration of generation-recombination centers and high crystallinity of ELA polysilicon films obtained by the SLS technique are inferred.

The investigation of the effect of illumination and the temperature dependence of the transient amplitude has indicated that hole emission, during the TFT ON state, is the dominant mechanism giving rise to drain current overshoot transients. The holes are generated from deep states in the device intrinsic body; those that escape recombination are captured during the OFF state and then reemitted during the ON state. At cryogenic temperatures the transient effects vanish out, as shown in fig. III.4.2, due to carrier freeze-out in deep states and exponential increase of generation lifetime. If illumination is present, electron-hole pair generation is enhanced, compensating the carrier freeze-out caused by the generation lifetime increase and leading to an extension of the transient behavior at low temperatures; thus the transient amplitudes remain high. Ascribing this behavior to hole emission rather than to electron capture better explains both the observed transient dependence on temperature and the influence of photo-excitation.



The transient signals at dark (fig. III.4.2) peak at a temperature T_m, shifting with the pulse width. For lower temperatures the transient amplitudes rapidly decrease. An Arrhenius plot of the T_m dependence on pulse width t_{OFF} (shown in fig. III.4.3) allows the determination of the activation energy E_A of the generation lifetime. The extracted value of 0.58 eV indicates that the defects acting as generation centers lie close to the middle of the silicon band gap.

Fig. III.4.2: *Temperature dependence of transient amplitude for different t_{OFF} durations.*

The value of the generation lifetime activation energy E_A could be used as a measure of the quality of the polysilicon films obtained by various techniques to various thicknesses. Finally, the temperature dependence of the quiescent drain current reveals, as shown in fig. III.4.3, an activation energy of 24 meV at dark and of 12 meV under illumination; this decrease under illumination is caused by the generated photovoltage across the barriers, which results in a decreased potential barrier height.

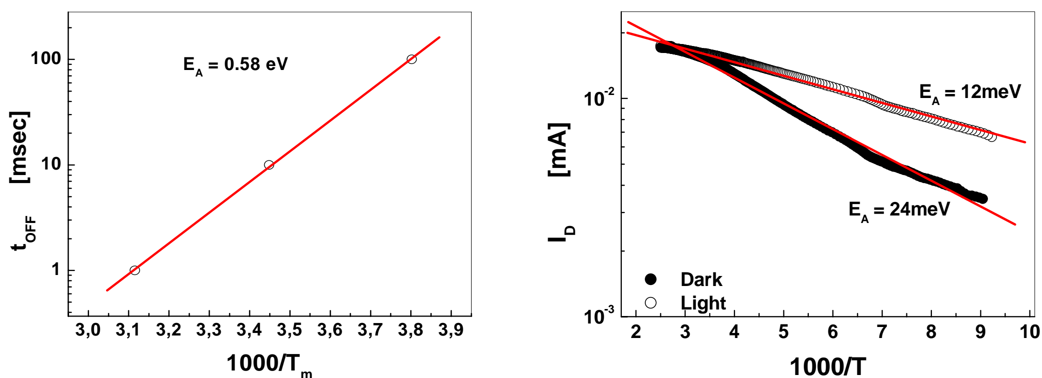


Fig. III.4.3: *Arrhenius plots of transient signal peak **(left)** and of quiescent I_D **(right)**.*

Task 3 Irradiation investigation

The degradation of the parameters of "directional" polysilicon SLS ELA TFTs under γ-irradiation was investigated and found to be more evident with increasing polysilicon film thickness and in the presence of a gate field during the irradiation. The extracted V_{th} and μ values are presented in fig. III.4.4. The γ-irradiation of these TFTs resulted in positive oxide charge trapping, inducing a negative V_{th} shift. The fact that the mobility was only slightly degraded indicates a good quality of the polysilicon – SiO_2 interface. The large V_{th} shift observed, which reaches 7 V at a dose of 700 Gy, indicates a high sensitivity of the PECVD gate oxide to γ-irradiation. Moreover, the charge trapping ΔN_{ot} in the oxide and ΔN_{it} at the interface was extracted using the shifts in the threshold and the midgap voltage ΔV_{th} and ΔV_{MG} (via the McWhorter – Winokur procedure), as shown in fig. III.4.4, and their increase with rising γ-irradiation dose was determined. It is evident that the irradiation-induced increases of the trapped charge densities ΔN_{ot} and ΔN_{it} are larger for TFTs fabricated in thicker polysilicon films.

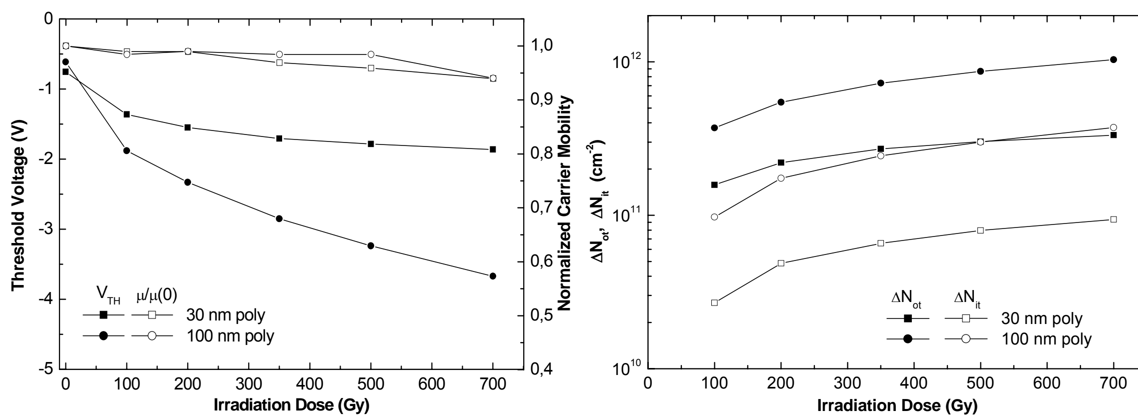


Fig. III.4.4: *V_{th} shift and μ degradation (left) and ΔN_{ot}, ΔN_{it} (right) vs. irradiation dose.*

Task 4 Polysilicon material characterization

The surface morphology and the grain structure of the polysilicon films are observed by means of SEM and AFM, while an investigation of the optical properties as a means for estimating the defectivity of the films has been initiated. The existence of a preferred direction for "directional" SLS ELA polysilicon films is evident from the SEM micrograph shown in fig. III.4.5.

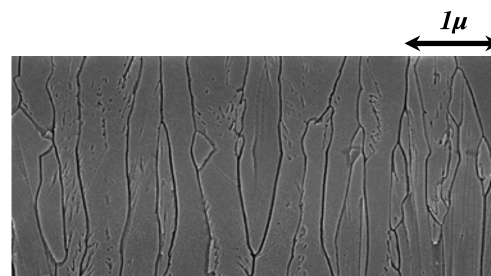


Fig. III.4.5: SLS ELA poly-Si film.

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. “On the switch-on overshoot transient decay mechanism in polycrystalline silicon thin film transistors”, Papaioannou, G.J., M. Exarchos, D.N. Kouvatsos and A.T. Voutsas, Applied Physics Letters, 87 (25), 252112, December 2005.
2. “Characterization of various low-k dielectrics for possible use in applications at temperatures below 160ºC”, Vasilopoulou, M., S. Tsevas, A.M. Douvas, P. Argitis, D. Davazoglou and D. Kouvatsos, J. of Physics: Conference Series, 10, 218, October 2005.
3. “Effects of DC gate and drain bias stresses on the degradation of excimer laser crystallized polysilicon thin film transistors”, Kouvatsos, D.N., L. Michalas, A.T. Voutsas and G.J. Papaioannou, Journal of Physics: Conference Series, 10, 45, October 2005.
4. “Deep Level Transient Spectroscopy Assessment of Drain Current Transients in Poly-Si Thin Film Transistors”, Exarchos, M.A., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, Journal of Physics: Conference Series, 10, 23, October 2005.
5. “The effect of Generation-Recombination mechanisms on the transient behavior of polycrystalline silicon transistors”, Papaioannou, G.J., A. Voutsas, M. Exarchos and D. Kouvatsos, Thin Solid Films 487 (1-2), 247, September 2005.
6. “Characterization of various insulators for possible use as low-k dielectrics deposited at temperatures below 200ºC”, Vasilopoulou, M., A. Douvas, D. Kouvatsos, P. Argitis and D. Davazoglou, Microelectronics Reliability 45 (5-6), 990, May 2005.
7. “Effect of silicon thickness on the degradation mechanisms of sequential-laterally-solidified polycrystalline silicon thin film transistors during hot-carrier stress”, Voutsas, A.T., D.N. Kouvatsos, L. Michalas and G.J. Papaioannou, IEEE Electron Device Letters EDL-26 (3), 181, March 2005.

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Effect of hot carrier stress on the performance, trap densities and transient behavior of SLS ELA TFTs”, Kouvatsos, D.N., G.J. Papaioannou, M. Exarchos, L. Michalas and A.T. Voutsas, Proceedings of the 35th European Solid State Device Research Conference (ESSDERC 2005), p. 395, Grenoble, France, September 2005.
2. “Thin film transistors fabricated in laser-crystallized chemically vapor deposited amorphous silicon films on quartz substrates”, Kouvatsos, D.N., A.T. Voutsas and G.J. Papaioannou, Proceedings of the 15th European Conference on Chemical Vapor Deposition (EuroCVD-15), Bochum, Germany, September 2005.

CONFERENCE PRESENTATIONS

1. “Characteristics of MOS diodes using sputter-deposited W or Cu/W films”, Tsevas, S., M. Vasilopoulou, D.N. Kouvatsos, A. Speliotis and D. Niarchos, Micro-and-Nano-Engineering 2005, Vienna, Austria, September 2005.
2. “Investigation of the temperature dependence of the electrical characteristics of polycrystalline silicon thin film transistors”, Michalas, L., G.I Papaioannou, D. Kouvatsos & A.T. Voutsas, 21st Panhellenic Conf. for Solid State Phys., Nicosia, Cyprus, Sept. 2005.
3. “Fabrication and characterization of MOS diodes with W or Cu/W gates deposited using sputtering”, Tsevas, S., M. Vasilopoulou, D.N. Kouvatsos, A. Speliotis and D. Niarchos, 21st Panhellenic Conference for Solid State Physics, Nicosia, Cyprus, September 2005.

M.Sc. THESIS

1. “Investigation of hot carrier effects in polycrystalline silicon TFTs”, Loukas Michalas, Physics Department, University of Athens, January 2005.