PROJECT III.5: CIRCUITS & DEVICES FOR OPTOELECTRONIC INTERCONNECTIONS

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- EU-STREP-IST PICMOS, Contract N^{o} 002131, 1/1/2004-31/12/2006
- OPTOELECTRONICS (ESA) - Multigigabit optical backplane for space applications, Contract N^{o} 17884, 5/1/2004-4/7/2005

Research orientation:

The main objective of the project is the development of the technologies for future high-density and high-speed optoelectronic interconnections. In order to accomplish this objective the additional specific targets of optoelectronic device modeling and simulation, implementation of optoelectronic technology in spacecraft environment as well as packaging in terms of photonic link integration above CMOS integrated circuits have been identified.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Development of a model for simulating Vertical Cavity Surface Emitting Lasers (VCSELs) and driving circuit topologies

Motivated by the fact that the ability to model VCSEL optical behaviour is critical to the design and analysis of optoelectronic micro-systems, we expand our proposed model scheme so that it will combine the non-linear behaviour of the input parasitics with the intrinsic fundamental device rate equations. The complete model for the VCSEL takes into account, by means of equivalent circuits the fundamental device rate equations, the thermal effects, the non-linear gain and transparency number functions and the input parasitic elements. A systematic methodology for the model parameter extraction from dc and ac, electrical and optical measurements is developed and extraction is achieved by a three-step procedure, which divides model parameters into distinct groups. Simulation results see fig. III.5.1a and b, using the proposed model, is compared with the experimental measurements and present satisfactory agreement. Simulation and extraction procedures are proved to be very fast while they preserve adequate accuracy.

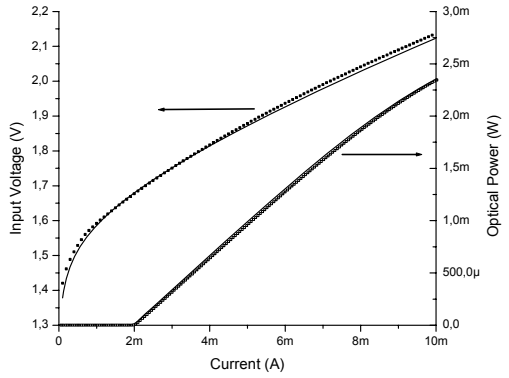

Fig. III.5.1a: *Measured values (dots) & simulated (continuous line) I-V & I-L characteristics at 20ºC*

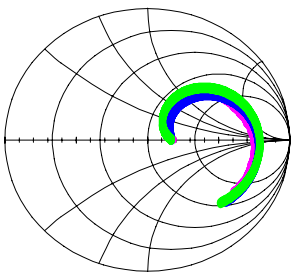

Fig. III.5.1b: *Measured values (pink line) @6mA & simulated s11 using parameters extracted @6mA & @4mA (blue & green line)*

Task 2 Multigigabit optical backplane for space applications

With the changing requirements in satellite operation it is important to assess how current developments in optical backplane interconnections can be applied to the next generation of spacecraft data handling and communication systems. This has been the goal of the ESA project 'Multigigabit optical backplane interconnections', in which we cooperate with IMEC of Belgium and Intune Technologies Ltd of Ireland.

Having chosen a wavelength routed star network architecture, based on an arrayed waveguide grating (AWG) router and tuneable transponders in the different nodes a demonstrator was developed. It consists of 4 nodes-of which only two have (for cost saving reasons) sending and receiving capability whereas the other two are only receivers-connected by an optical backplane. The demonstrator basically consists of three parts: the wavelength router, the transponders and the nodes generating or receiving data and implementing the control plane.

- The passive wavelength router transparently implements the network functionality on the physical level. The router has two input ports and four output ports, optically connected to laser and detector ports of the transponders. The router can support unicast and multicast links between inputs and outputs. The wavelength used by a sender determines the receiver of the data sent. A 4x4 AWG has been developed in silicon-on-insulator (SOI) technology, for compactness, and used in the demonstrator.
- The transponder cards contain tuneable transmitter and fixed (APD and PIN based) receiver modules capable of sending and receiving 10Gbps data streams. The transponders are equipped with tuneable laser diodes, which have been equipped with external modulators and control electronics. These lasers have 80 50GHz-spaced wavelength channels from 1528nm to 1563 nm. The switching time for these units is below 100ns for a selected subset of the 80 supported wavelength channels.
- Each transponder communicates electrically with a data and control node that generates 10Gb/s data streams. The nodes also take care of the medium access control using predefined communication schemes locally stored in routing tables on every node. One node acts as the master and provides synchronisation signals to all other nodes in order to change simultaneously to the next backplane configuration. Additionally, all nodes can communicate with a PC. Our work is focused on the protocol aspects of the backplane as well as the design and implementation of the control unit using high-speed FPGAs. In fig. III.5.2 the four-node demonstrator set-up is shown.

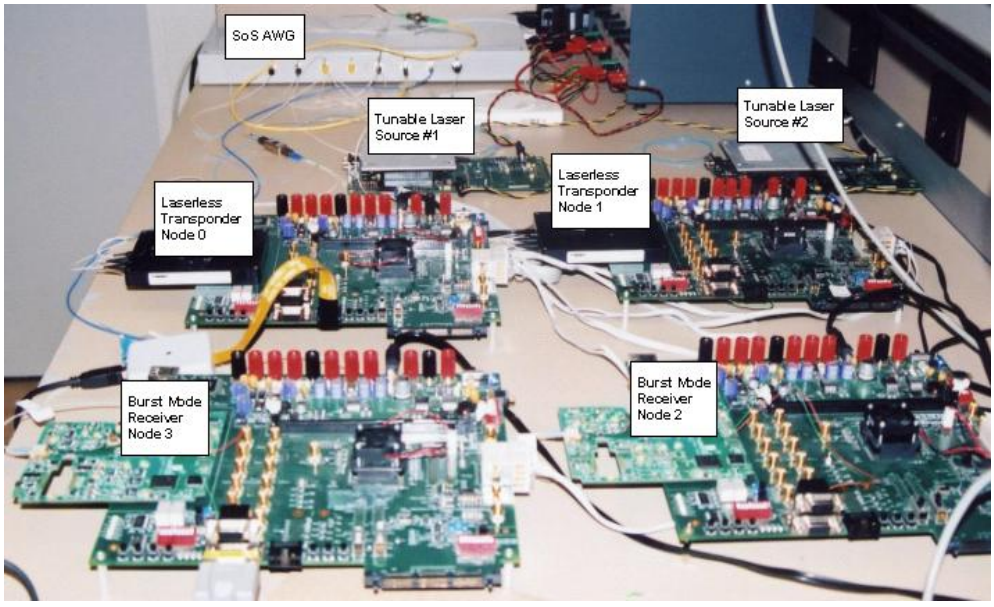

Fig. III.5.2: The Demonstrator Photograph shows the AWG and the 4 nodes: 2 laserless transponders with tuneable laser sources & two burst mode receivers. The four nodes are shown as node 0 to node 3.

Task 3 Heterogeneous integration of optical interconnects onto CMOS ICs

Photonic dies with fully integrated optical paths-sources and detectors coupled to waveguides-are bonded onto a CMOS integrated circuit (IC). The metallic bonding technique that is used utilizes a thin multilayer structure of the Au-20Sn eutectic alloy along with a thin starting layer of rare earth Gd and contains versatile structures for passive alignment. Its main advantage is the fact that it accomplishes mechanical bonding and electrical connectivity in a single step. Pattern uniformity, limited alloy spreading and contact resistance in the mΩ range across a 4-inch wafer allow for dense CMOS/photonic integration. Fig.III.5.3 shows an array of 3x4 dies attached to a 4in wafer. This project is executed in collaboration with IMEC, Belgium, ST, CEA, CNRS-FMNT, France, and TUE, Holland, in the framework of the European project PICMOS.

Fig. III.5.3: *Four-inch wafer with multiple dies bonded on specific regions.*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS

1. “Driving High Speed VCSELs”, K.Minoglou, E.D. Kyriakis-Bitzaros, S.G.Katsafouros, D. Syvridis, G. Halkias, Microwave and Optical Technology Letters (Vol 44, Issue 1, January 2005, pp. 41-45)

INVITED TALKS

1. “System level modeling and simulation of optical interconnects”, E.D.Kyriakis-Bitzaros, K.Minoglou and G.Halkias, Invited Talk, ECIO’05, 12th European Conference on Integrated Optics, Grenoble, April 6-8 2005, pp.335-344

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Metallic bonding of optoelectronic dies to silicon wafers”, K.Minoglou, E.D.Kyriakis-Bitzaros, E.Grivas, S.Katsafouros, A.Kostopoulos, G.Konstadinidis and G.Halkias, Journal of Physics:Conference series 10 (2005), pp.393-396

ANNEX I

RESEARCH PRODUCTS OF IMEL

a) Lithography and plasma etching software

- Software for line-edge-roughness (LER) measurement and characterization from SEM images.
- Software for nanolithography simulation and LER prediction based on Monte Carlo methods.
- Software for topography evolution simulation during plasma processing.

b) MEMs devices

Flow sensors

Using porous silicon micro-hotplate technology, different gas and liquid flow sensors were developed at IMEL. The proprietary gas flow sensor of IMEL using local thermal isolation on silicon either by a compact porous silicon layer or a porous membrane over a cavity, shows superior characteristics compared with other existing devices in the literature.
A system for respiration control using the above flow sensor has been designed and fabricated at IMEL which works quite linearly in a large flow range from -200 to +200 slpm. The system shows important advantages compared with existing systems in the commerce (high sensitivity, low cost, linearity, fast response). Modeling and simulation were used to optimize the sensor and housing design.

Thermal accelerometer based on porous silicon technology for thermal isolation

A silicon accelerometer without solid proof mass has been developed and characterized, based on the thermal sensor developed at IMEL. The device was tested in a specially designed vibration system for different frequencies and acceleration values. It shows important advantages over existing systems also for this application, when used in a fluid medium.

Porous-silicon-sealed microchannels on a silicon substrate

A two-step electrochemical process has been developed for the fabrication of sealed air cavities or capped micro-channels on a silicon substrate. The capping material is a porous silicon membrane which is planar to the silicon substrate. Two interesting applications of this technology are targeted: a) The effective local thermal isolation on a silicon wafer for use in micromachined thermal sensors, b) The potential use of this technology in the fabrication of microfluidic devices. Research in this direction is related with the design, modelling, fabrication and characterization, using the above process.

c) Bio - MEMs

A bioanalytical lab-on-a-chip device based on monolithic optoelectronic transducers has been developed at IMEL (see project III.3).