Project II. 1: NANOSTRUCTURES FOR NANOELECTRONICS AND PHOTONICS

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- EU IST NoE SINANO, 1/1/2004-31/12/2006, Contract N^{o}: 506844
- EU IST NoE MINA-EAST, 1/5/2004-30/4/2006, Contract N^{o}: 510470

Research orientation:

- Fabrication and characterization of semiconductor nanostructures (quantum wires, quantum dots, optical properties, charging effects, self-assembling, ordering) and theirs applications in non-volatile memories and photonic devices
- Fabrication and characterization of anodic porous alumina on silicon and its use in nanofabrication
- Self-assembled building blocks for nanoelectronics (self-assembly of nanoparticles, application in nanoelectronic devices, transport properties)
- Thermal transport in nanostructures

The activity on semiconductor nanostructures started at IMEL at the early nineties, within the framework of the Esprit project EOLIS (1992-1996) (pioneering work at IMEL on silicon nanopillars) and continued within the EU projects IST FET SMILE, contract No 28741, IST FORUM FIB, contract No 29573, and continues at present within the EU projects IST NoE SINANO and IST NoE MINA-EAST. The focus is on quantum dots and wires and their use in emerging electronic (e.g. nanocrystal memories) and photonic devices.

The activity on self assembly started at IMEL within the EU project IST FET Escher, contract No 33 287. In general, the concept of self-assembly has become very popular the last years, because it offers a possible way for creating potentially useful structures of the size of few nanometers or tens of nanometers. Self-assembly is seen as a good candidate for a new fabrication technology for the future information processing devices. IMEL is involved in the investigation of Au nanoparticles self-assembled between electrodes by dielectrophoresis and their use in bio-sensing.

Another interesting activity concerns anodic porous alumina thin films on silicon. A lot of work has been devoted in the literature to anodic porous alumina on bulk aluminum. Free standing porous alumina membranes with very regular pores vertical to the surface are fabricated and used in diverse applications, as for example in nanoparticle filters. More recently, porous alumina thin films are fabricated on a silicon substrate by anodization of Al thin films. They are used either as templates for the growth of different nanostructures through the pores (nanowires, quantum dots), or as matrices for the fabrication of composite materials. Very thin alumina films were fabricated on silicon at IMEL, with very regular vertical pores, which are very appropriate for the development of different nanopatterning and self-assembly techniques.

Thermal transport in nanostructures is a theoretical activity with important impact on applications in sensors. It is carried out in collaboration with research scientists of programme III.

Main results in 2005

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 LPCVD growth of double-layers of silicon nanocrystals within the gate dielectric of a MOS structure for improved non-volatility in nanocrystal memories

A Salonidou and A. G. Nassiopoulou
In collaboration with K. Giannakopoulos and A. Travlos from the Institute of Materials Science for TEM work

Layers of silicon nanocrystals embedded in SiO_2 are fabricated in this work by low-pressure chemical vapor deposition (LPCVD) of amorphous Si, followed by high temperature oxidation. The thickness of the amorphous layer as well as the oxidation time is adjusted so as to get the desired thicknesses of the nanocrystal layer and the top oxide. This process shows the advantage of controllable nanocrystal size and a good quality barrier silicon oxide.

By using the above process, single and double layers of silicon nanocrystals were fabricated within the gate dielectric of a MOS memory structure. Double layers were found to improve substantially the retention characteristics of the memory.

Fig. II.1.1. shows TEM images of two samples (Z_2 (a) and L (b)) with double layers of Si nanocrystals. In sample L the two nanocrystal layers are close together, their inter-distance being equal to 1.5nm, and they are situated at a tunneling distance from the silicon substrate. The lower layer, close to the substrate, is composed of smaller dots (d=3nm) than those of the upper layer (d=5nm). In sample Z_2 the dot layers are composed of dots of equal diameter (d=3nm) and their inter-distance is much larger (13nm). In both cases, the retention characteristics of the structure are improved compared with a single dot layer structure. In the second case this improvement is significantly larger than in the first case; almost no charge loss was measured after 10^4s from writing time.

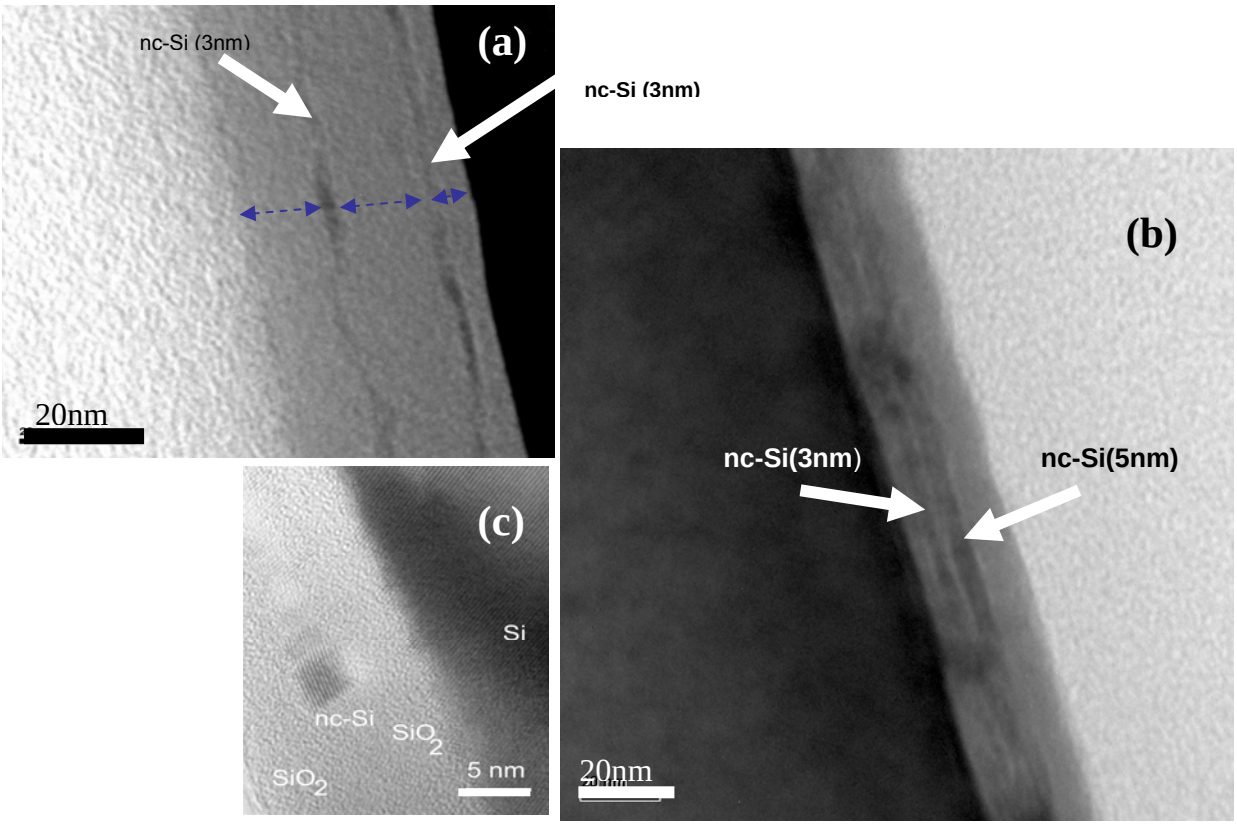
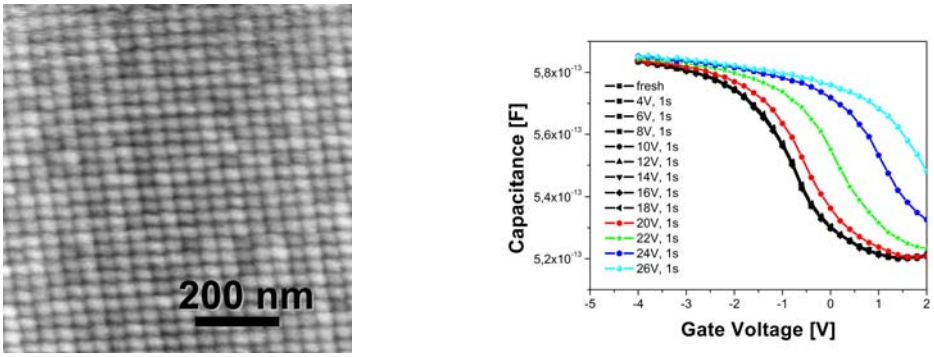


Fig. II.1.1: *Dark field TEM images of samples Z_2 and L with a double layer of silicon nanocrystals within SiO_2. In sample Z_2 (a) the gate stack is: SiO_2 (13nm)/Si-nc, d≈3nm/SiO_2-13nm/Si-nc, d≈3nm/SiO_2 (tunneling) 3,5nm/p-type Si substrate. In sample L (b) the gate stack is: SiO_2-8nm/ Si-nc, -d≈5nm/SiO_2-1,5nm/Si-nc, d≈3nm/SiO_2 - 3,5nm/p-type Si substrate. In (c) we see a high resolution dark field image of one nanocrystal of sample Z_2.*

Task 2 Ge dots in thin SiO_2 layers for application in non-volatile memories

A. Olzierski, E. Tsoi and A. G. Nassiopoulou

The use of Ge dots in a two-dimensional layer within SiO_2 as the charging medium in a MOSFET non volatile memory cell shows advantages compared with silicon nanocrystal NVMs. Due to the valence band offset between Ge dots and the Si substrate, better retention characteristics for holes compared with those achieved with silicon nanocrystals are expected. This approach is often described as dot storage engineering. Within this task, the growth of Ge nanocrystals in thin SiO_2 layers was studied and processes were developed, which include the fabrication of ordered and randomly distributed Ge dots in two-dimensional layers in SiO_2.



(a) **(b)**

Fig. II.1.2: ***(a)*** *AFM image of ordered Ge dots fabricated by FIB pre-patterning of the silicon surface, thermal oxidation to grow the tunnel oxide and dot growth by MBE.* ***(b)*** *Capacitance-Voltage characteristics of a capacitor using the ordered Ge dots within the gate dielectric.*

For the lateral ordering of the Ge dots, the combination of the following technological steps was used, in collaboration with $CRMC_2$ in France: a) use of a focused ion beam (FIB) to create ordered two-dimensional arrays of regular holes on a field oxide on the silicon substrate, b) chemical cleaning and restoring of the Si surface in the holes, c) further oxidation to transfer the pattern from the field oxide to the silicon substrate, d) removal of the field oxide and thermal re-oxidation of the sample in order to create a tunnel oxide of homogeneous thickness on the patterned silicon surface and c) self-assembly of the two-dimensional arrays of Ge dots on the patterned tunnel oxide. For the completion of the process and the fabrication of test structures (capacitors), a TEOS oxide was used as the control oxide (see fig II.1.2). Efficient charging of the structure by electron injection from the silicon substrate was demonstrated, resulting in a significant shift of the flat-band voltage of the MOS capacitor.

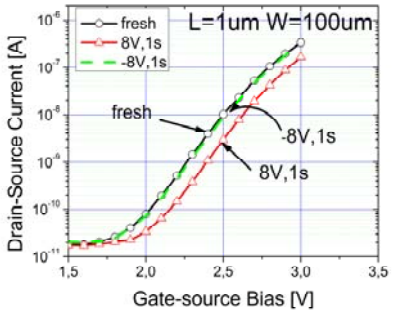


Fig. II.1.3: *I_{ds}-V_{gs} characteristic of the fabricated memory cell with non-ordered Ge dots.*

Randomly distributed Ge dot memory cells were also fabricated using e-gun evaporation of Ge on a tunnel SiO_2 layer, followed by TEOS deposition as the control oxide and rapid thermal annealing treatment at 1000°C for 250s. These cells demonstrate memory effect with a memory window of ~ 0.15 eV with write/erase voltages of +8 V, 1 s/-8 V, 1 s (see fig. II.1.3).

Task 3 Very thin anodic alumina templates on silicon for nanofabrication

M. Kokonou and A. G. Nassiopoulou

Porous anodic alumina is an extensively studied material due to its unique, self-organized structure that resembles a honeycomb. The last decade it has received additional attention due to its potential use as a masking or template material for the growth of nanowires and nanodots. For the fabrication of arrays of nanodots on silicon, it is highly desirable to reduce to the minimum the alumina template thickness, in order to facilitate dot growth through the pores and to have better and more accurate control on dot size and shape.

Within this task, anodic porous alumina films with thickness in the range of 20 to 50 nm were fabricated on a silicon substrate by electrochemistry, for use as templates for silicon nanopatterning and quantum dot growth. The anodization conditions were investigated in detail and it was found that they differ significantly from those used to grow thicker films. Much lower electric fields were necessary, since the strong electric field causes fast dissolution of the grown alumina. Anodization was done in sulfuric or oxalic acid aqueous solutions. Due to the low anodization voltage used, high density of pores was achieved. By using the optimum anodization conditions found, anodic porous alumina films on silicon with small diameter high density vertical pores homogeneously distributed in the film were fabricated and characterized by transmission electron microscopy.

Regular arrays of stoichiometric SiO_2 dots were grown on silicon through the pores of anodic porous alumina, during the same anodization process used for alumina formation. The SiO_2 dot diameter increases by increasing the anodization time and the dots merge together for excessively long times. By extensive characterization using AFM and TEM it was concluded that for short oxidation times after initiation of silicon oxidation a lower SiO_2 dot density is obtained (dot density is smaller than pore density), while many dots are at an inception stage. The height of the dots rapidly increases after nucleation, reaching values in the range of 8-10 nm. At long oxidation times dots continue to nucleate up to the pore density. The already nucleated dots increase in height and width, as resulted from AFM images, reaching saturation values at about 14 nm in height and 60 nm in width. From XPS and EELS spectra it was verified that the silicon oxide of the dots was stoichiometric SiO_2.

Fig. II.1.4 shows on the left the anodization current density versus time during anodization for alumina growth, with subsequent SiO_2 dot growth at the pore tips. The vertical dotted line shows the point where the Al is fully consumed and the oxidation of the silicon substrate starts at each pore tip. In (a) we see a plan view TEM image of the alumina film and in (b) and (c) we see respectively AFM and EELS images of the SiO_2 dots, after removal of the alumina film.

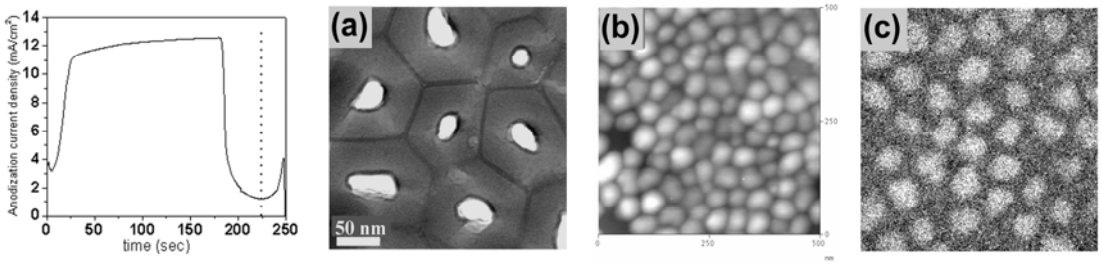
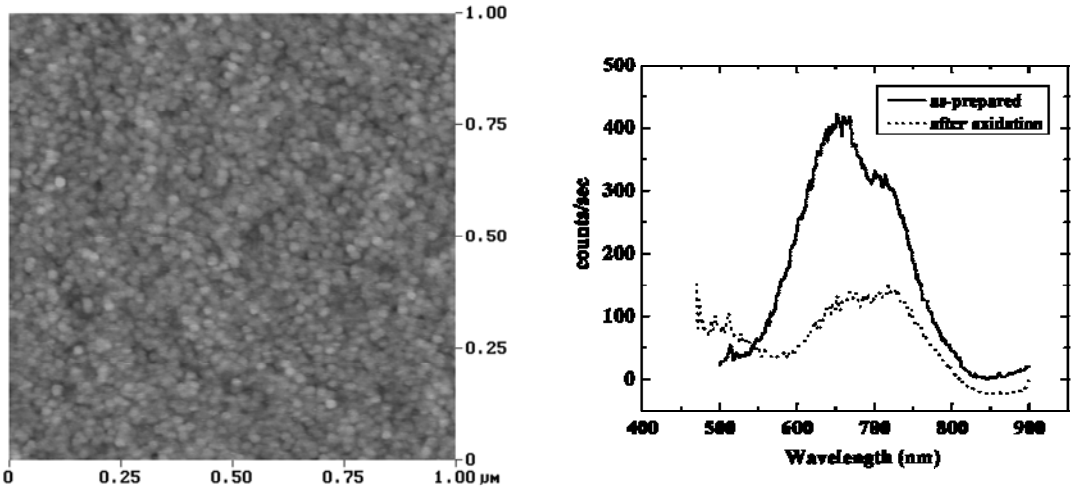


Fig. II.1.4: *The diagram on the left shows the anodization current density versus time. The vertical dotted line shows the point where the Al is fully consumed and the oxidation of the silicon substrate starts at each pore tip.* ***(a)*** *plan view TEM image of a nanoporous alumina film.* ***(b)*** *AFM image of arrays of SiO_2 nanoislands obtained by anodic oxidation through the pores of the alumina layer.* ***(c)*** *Oxygen mapping of the dots by electron energy loss spectroscopy (EELS) in a TEM.*

Task 4 Growth of silicon nanocrystals embedded in silicon dioxide for optoelectronic applications

S. Gardelis and A. G. Nassiopoulou

In this work we have grown silicon nanocrystals by anodization of bulk crystalline silicon in the transition regime using extremely short pulses (of few hundreds milliseconds duration) of anodic current in hydrofluoric acid- based solutions. This method produces a highly dense two-dimensional array of silicon nanocrystals isolated from each other as can be seen in the AFM image shown below (fig. II.1.5a). A typical size of these nanocrystals is 2.5-3 nm. Efficient photoluminescence was observed at room temperature peaked typically at 600-650 nm (fig. II.1.5b), originating from the silicon nanocrystals. After controlled oxidation of the layers in dry oxygen atmosphere at 850^{o}C we managed to obtain silicon nanocrystals embedded in silicon dioxide, as the Fourier Transform Infra Red (FTIR) measurements demonstrate. The nanocrystals continue to emit in the red, however with reduced intensity compared to those in as-grown samples, whereas a second luminescence band peaked at 500 nm appears (fig.II.1.5b). This band shows a fast decrease in the intensity under laser illumination and originates from oxide-related defects. This growth method could be proved a cheap method to produce silicon nanocrystals for optoelectronic applications.



(a) (b)

Fig II.1.5: ***a)*** *AFM image of a two-dimensional array of silicon nanocrystals formed by anodization of crystalline silicon using extremely short pulses of anodic current.* ***b)*** *Photoluminescence spectrum before and after oxidation.*

Task 5 Thermal transport in nanostructures

N. Papanikolaou

Heat transport in nanostructures like quantum dot arrays, multilayers, and nanowires show new interesting properties that do not exist in the bulk materials. In semiconductors, heat is transferred mainly by lattice vibrations. We use atomistic classical molecular dynamics simulations to study the thermal conductivity of SiC nanowires with diameter of a few nanometers. The atomic interactions are modeled by the Tersoff potential which can give a reasonable description of the lattice dynamics of SiC. Thermal conductivity is calculated by the so called non-equilibrium method. Heat is added and removed in two different positions of the wire by rescaling the velocities of the atoms. The resulting temperature gradient is used to calculate the thermal conductivity using Fourier law. Thermal conductivity is greatly reduced compared to the bulk while heat transfer is influenced by the diameter as well as the termination of the nanowires.

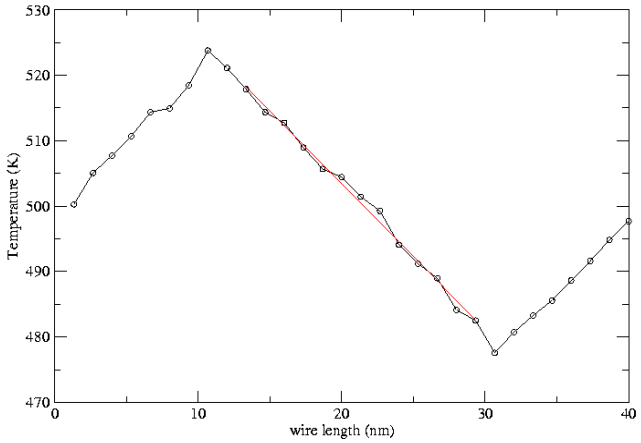


Fig. II.1.6: *Temperature gradient for a C terminated SiC wire of 4 nm diameter. Heat is added (removed) at around 10 (30) nm. The resulting profile is almost linear and it is an average over 800000 molecular dynamics steps.*

Phonon scattering at the wire surface is the main factor responsible for the reduction of the thermal conductivity. We plan to extend our study to include structural and chemical defects in the wires as well as study phonon scattering at interfaces of multilayer structures.

Task 6 Self assembly of gold nanoparticles by dielectrophoresis

A. Zoy and A.G. Nassiopoulou

In this work we develop the dielectrophoresis technique for controllable and rapid assembly of nanostructures between electrodes. This technique is based on the force exerted on the induced dipole moment of a dielectric or conductive particle by a non-uniform electric field. Alternative (AC) electric fields are often preferred in order to suppress electrochemical reactions, as for example electrolysis at the electrodes surface and to overcome the limitation of strong surface particle charge. DEP is suitable for microfluidic applications and nanoassembly.

At IMEL, dielectrophoresis is used for the controllable assembly of gold nanoparticles between electrodes and the formation of conductive nanowires with micrometer length. Different aqueous colloidal gold nanoparticles with average diameter of 20, 30, 40 and 45 nm were assembled between gold or platinum electrodes with 1 μm distance placed on a 150 nm thick SiO_2 layer. The effect of the frequency and strength of the applied field on the particle accumulation process was investigated. Two typical results at low and higher frequency including SEM images and corresponding current-voltage characteristics are shown in fig.II.1.7.

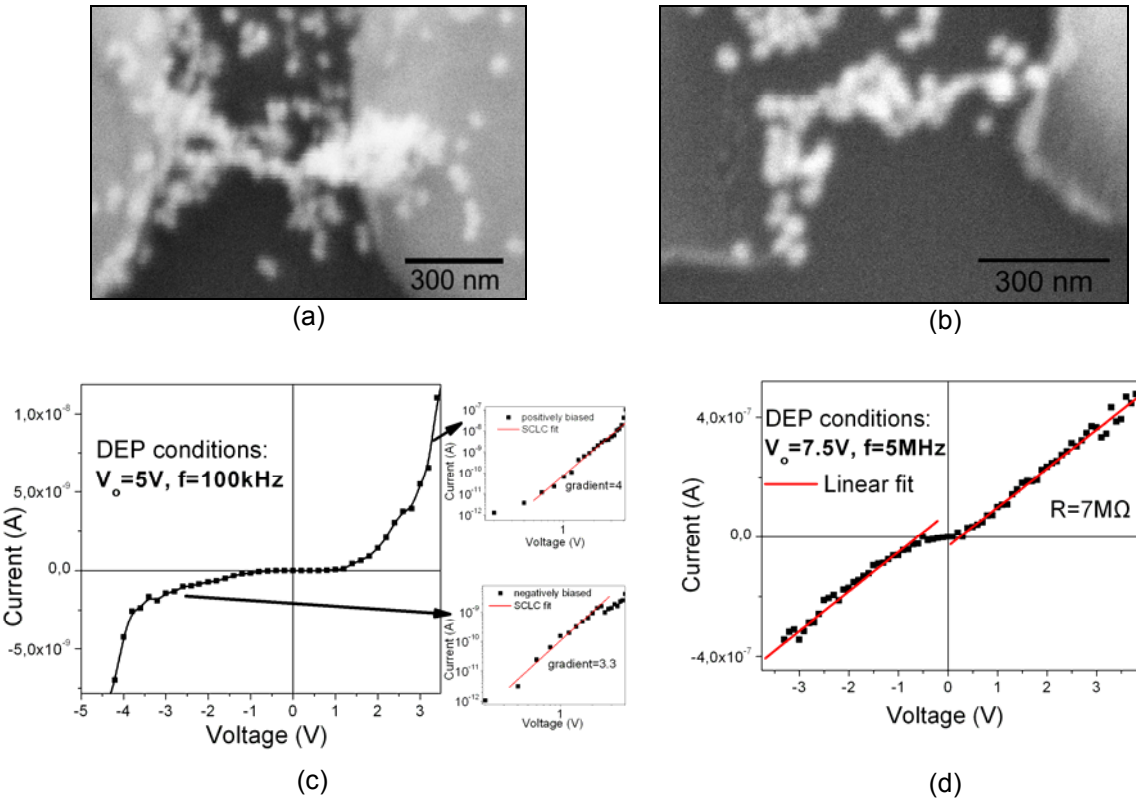


Fig. II.1.7: *Two examples of nanowires formed between triangular Pt electrodes, using an AC field with* ***(a)*** *amplitude 5 V and frequency 100 kHz,* ***(b)*** *amplitude 7.5 V and frequency 5 MHz and* ***(c)*** *and* ***(d)*** *example of current-voltage characteristics of these structures.*

At low frequencies, the Au nanoparticles are aggregating as shown in the SEM image of a sample deposited with 5V voltage amplitude at 100 kHz in fig. II.1.7a. The corresponding I-V characteristic (fig. II.1.7c) is polynomial, which is indicative of space charge limited conductivity of the structure. Both parts of the I-V curve are presented in log-log scale in the inserts. At higher frequencies, the Au nanoparticles are deposited in a discrete way as shown in fig. II.1.7b (5 MHz). This sample exhibits a linear conductivity with the applied voltage in the range -3 to +3V, with a resistance of 7 MΩ, which is indicative of hopping transport between the Au nanoparticles.

PROJECT OUTPUT in 2005

PUBLICATIONS in REFEREED JOURNALS

1. “Structural study of very thin anodic alumina films on silicon by anodization in citric acid aqueous solution”, M. Kokonou, A. G. Nassiopoulou, K. G. Giannakopoulos, N. Boukos, A. Travlos, J.Nanoscience and Nanotechnology v.5, 1-5, 454-458, (2005)
2. “Ultra thin porous anodic alumina films with self-ordered cylindrical vertical pores on a p-type silicon substrate”, M. Kokonou, A. G. Nassiopoulou & K. P. Giannakopoulos, Nanotechnol. 16, 103, (2005)
3. "Optical properties of Si quantum wires and dots", X. Zianni and A. G. Nassiopoulou, Review Paper, Handbook of Theoretical and Computational Nanotechnology, edited by Michael Rieth and Wolfram Schommers, American Scientific Publishers, vol. 1 chapter 94, pages 1-37, (2005)
4. "Optical emission behavior of Si quantum dots", X. Zianni and A. G. Nassiopoulou, in "Quantum dots: Fundamentals, Applications and Frontiers" edited by: B. A. Joyce et al., NATO Science Series II. Mathematics, Physics and Chemistry, vol. 190, pages 369-376 (2005)
5. “Thin porous anodic alumina films: Interface trap density determination”, M. Theodoropoulou, P. K. Karahaliou, S. N. Georga, C. A. Krontiras, M. N. Pisanias, M. Kokonou, A. G. Nassiopoulou, IONICS, 11 (3-4): 236-239 2005

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Silicon nanocrystal memories by LPCVD of amorphous silicon, followed by solid phase crystallization and thermal oxidation”, E. Tsoi, P. Normand, A. G. Nassiopoulou, V. Ioannou-Sougleridis, A. Salonidou and K. Giannakopoulos, J. Phys.: Conf. Ser. 10 31-34 (2005)
2. “Charging characteristics of Si nanocrystals embedded within SiO_2 in the presence of near-interface oxide traps”, V. Ioannou-Sougleridis and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 39-42 (2005)
3. “Two-dimensional arrays of ordered, highly dense and ultra-small Ge nanocrystals on thin SiO_2 layers”, I. Berbezier, A. Karmous, A. Ronda, T. Stoica, L. Vescan, R. Geurt, A. Olzierski, E. Tsoi and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 73-76 (2005)
4. “Electrical conductivity of Au-nanoparticle-coated K_2SO_4 microcrystals deposited by DC trapping”, A. Zoy, A. G. Nassiopoulou, V. Ioannou-Sougleridis, M. Murugesan and B. D. Moore, J. Phys.: Conf. Ser. 10 105-108 (2005)
5. “Nanotemplate alumina films on a silicon substrate fabricated by electrochemistry”, M. Kokonou, A. G. Nassiopoulou, K. P. Giannakopoulos and N. Boukos, J. Phys.: Conf. Ser. 10 159-162 (2005)
6. “Interface traps density of anodic porous alumina films of different thicknesses on Si”, M. Theodoropoulou, P. K. Karahaliou, S. N. Georga, C. A. Krontiras, M. N. Pisanias, M. Kokonou and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 222-225 (2005)
7. “Ultrafast carrier dynamics in highly implanted and annealed polycrystalline silicon films”, E. Lioudakis, A. G. Nassiopoulou and A. Othonos, J. Phys.: Conf. Ser. 10 263-266 (2005)
8. “Semiconductor nanocrystals in thin SiO_2 layers for non-volatile memories”, A. G. Nassiopoulou, A. Salonidou, A. Olzierski, M. Kokonou, E. Tsoi, P. Normand, K. Giannakopoulos, Proceedings of the International workshop on semiconductor nanocrystals (SEMINANO) held in Budapest, September 10-12, 2005, p.p. 405-410 (2005)

PRESENTATIONS in CONFERENCES

1. “Self assembly of colloidal gold nanoparticles in-between micrometer electrode gaps by dielectrophoresis”, A. Zoy, A. G. Nassiopoulou, M. Murugesan andB. D. Moore, XXI Panhellenian Conference on Solid State physics and Materials Science, Nicosia, Cyprus 28-31 August 2005
2. “Arrays of SiO_2 nanoislands grown electrochemically on Si through nanoporous anodic alumina”, M. Kokonou, A. G. Nassiopoulou and K. P. Giannakopoulos, 3rd International Symposium on Nanomanufacturing (ISNM 2005), Nicosia, Cyprus, November 3-5, 2005

INVITED TALKS-LECTURES

1. “Silicon nanocrystals in thin SiO_2 layers for light emission and nonvolatile memories”, A. G. Nassiopoulou, (invited talk), First International Workshop on Semiconductor Nanocrystals (SEMINANO 2005), September 10-12, 2005, Budapest Hungary
2. “New challenges in nanoelectronics and sensors”, A. G. Nassiopoulou, (invited talk), WSEAS International Conference on Engineering Education, July 8-10, 2005, Athens, Greece
3. “From Micro to Nanoelectronics and Nanotechnology: Contribution to Society and National Economies”, A. G. Nassiopoulou (invited talk), Workshop on “Physics and the other Sciences”, Thessaloniki, 9 December 2005
4. "From Micro to Nanoelectronics and Nanotechnology: a revolutionary development", A. G. Nassiopoulou (invited talk, award of honorary plaque), Workshop on Micro and Nanoelectronics", TEI Lamias, 18 May 2005
5. “Nanotechnology at IMEL with applications in ICT, Health Care and Environment”, A. G. Nassiopoulou, Workshop: “NCSR Demokritos in a knowledge-based society”, Zappio, 6 July 2005