Project II.2: NANOCRYSTAL MEMORIES

Project leader: Dr P. Normand

Key Researchers: Dr P. Normand, Dr V. Ioannou-Sougleridis

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PhD candidates: P. Dimitrakis, E. Kapetanakis, S. Kolliopoulou

Main External Collaborators in 2005: Prof. D. Tsoukalas (NTUA), Dr C. Bonafos and Dr G. BenAssayag (CEMES/CNRS), Dr B. Schmidt (FZR), Dr M. Petty (Univ. Durham), Dr A. Nylandsted (Univ. Aarhus)

Objectives:

- To develop novel high-throughput synthesis routes and techniques for creating nanoparticles in dielectrics, such as silicon nanocrystals in SiO_2 films by low-energy ion-beam-synthesis.
- To investigate the structural and electrical properties of the generated nanostructured materials and demonstrate material characteristics enabling the development of low-voltage high-density memory devices.
- To realize and evaluate nanostructure-based-memory devices and assess the manufacturability of the developed nanofabrication routes in an industrial environment.

Research orientation:

By associating the finite-size effects (e.g. Coulomb blockade) of nanocrystals and the benefits (robustness and fault-tolerance) of a stored charge distribution, the nanocrystal memories (NCMs) offer an attractive alternative for extending the scaling of conventional floating-gate memories (e.g. Flash EEPROMs). Our activities in this area started in 1996 through the development of the low-energy ion-beam-synthesis (LE-IBS) technique for producing nanocrystals in thin gate dielectrics. In collaboration with the University of Salford and the University of Thessalonique, generation of a 2D-array of Si nanocrystals in SiO_2 films by LE-IBS was demonstrated in 1997. This activity was further supported by the EU project, FASEM (1997-2000). LE-IBS Si-NCMs with endurance and write/erase times that approach those of DRAM were demonstrated in 1999. Observations of room-temperature single-electron storage effects in large-area n-channel Si-NC-MOSFETs were reported for the first time in 2002. Development of the LE-IBS technique with target the realization of manufactory non-volatile NCMs, has been conducted within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last three years to the development of novel NCMs alternatives including, (a) Memory devices by Si^+ irradiation through poly-Si/SiO_2 gate stack in collaboration with Research Center Rossendorf and Zentrum Mikroelektronik Dresden, (b) Memory devices using Ge nanocrystals produced by molecular-beam epitaxy and rapid-thermal processing in collaboration with Aarhus University, (c) hybrid silicon-organic and SiGe-organic memories in collaboration with the University of Durham; this last activity was initiated within the framework of the EU IST-FET project, FRACTURE (2001-2003).

In 2005, the main focus in our activities was on the following four tasks:

1. Low-voltage Si nanocrystal memories obtained by low-energy ion-beam-synthesis
2. Channel edge effects in shallow-trench-isolated nanocrystal memories
3. Hybrid SiGe/organic MOSFET with self-assembled Au-nps for memory applications
4. Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride

Specific targets for 2006 include: (a) Fabrication of Si NCs of controlled size and interspacing by block-copolymer-assisted-nanopatterning in collaboration with project I.1, (b) development of a novel Si-NC synthesis route based on plasma-immersion ion-implantation in collaboration with CEMES/CNRS and one French SME (Ion Beam Services), (c) formation of oxide/nitride/oxide dielectric stacks with Si-NCs embedded in the nitride layer by LE-IBS and LPCVD for achieving fast memory devices with improved non-volatility.

Main results in 2005

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Low-voltage Si nanocrystal memories obtained low-energy ion-beam-synthesis

P. Dimitrakis, E. Kapetanakis, D. Tsoukalas, P. Normand

The realization of LE-IBS Si-nanocrystals into SiO_2-gate dielectrics for low-voltage non-volatile memory devices, is not trivial for two main reasons. First, the LE regime (typically around 1keV) does not allow the production of structures with asymmetrical oxide barriers such as the control oxide (CO) above the NC layer is thicker than the injection or tunnel oxide (TO). Second, the implantation doses required for NC fabrication severely damage the host matrix and efficient oxide healing using reasonable post-implantation annealing conditions remains a difficult task. A technical option to overcome these issues is based on post-implantation thermal treatments in nitrogen-diluted-oxygen ambient. Such an alternative results from a compromise between several requirements: (1) to keep a moderate thermal budget, (2) to form a high-density of separated and passivated NCs, (3) to enhance the insulating properties of the control oxide and obtain functional asymmetrical barriers. This can be achieved under slight oxidizing annealing conditions that should be carefully adjusted according with the implantation parameters.

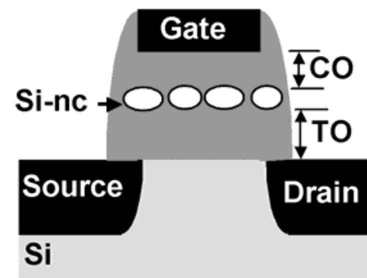

Fig. II.2.1: *A schematic cross-section of a nanocrystal memory device.*

In this direction, our 2005-activities have been concentrated first, on the thermal oxidation in N_2-diluted-O_2 of high-temperature pre-formed silicon NCs in collaboration with CEMES/CNRS (FR) and second, on the effect of the annealing duration and N_2/O_2 composition on the memory performance of Si-implanted-SiO_2 gate dielectrics. This last study is important not only to demonstrate that annealing in N_2/O_2 may provide a potential solution for generating functional LE-IBS NC gate dielectrics, but also to investigate if such an alternative can lead to a reliable process window. For this purpose, 7nm-thick SiO_2 oxides were implanted with 1keV Si ions to a dose of $2x10^{16}$ cm^{-2} and subsequently annealed at 950°C for 30 min in N_2/O_2 mixtures with oxygen contents ranging from 1 to 5%.

Typical memory windows obtained after application of 100ms symmetrical positive and negative gate pulses are presented in fig. II.2.2. For oxygen contents higher than 2%, the memory effect is dramatically reduced and almost disappears for the 5% O_2 regime. The attainable memory windows (~ 2V) are quite similar for the 1, 1.5 and 2% O_2 regimes while charge injection occurs at lowest voltages for the lowest O_2 content. This result is mainly attributed to injection oxide healing that reduces significantly the conductivity of the oxide and thereby, the trap-assisted-mechanism involved in NC charging. It should be noted here that any change in oxide conductivity affects the charge retention properties of the NC gate dielectrics and therefore, the best process window should result from a compromise between programming regime (voltage and speed) and retention time. Memory behavior of the above implanted oxides after annealing at 950°C in 1.5% O_2 for a duration ranging from 5 to 120min is reported in Tsoukalas et al., MSE B, 2005.

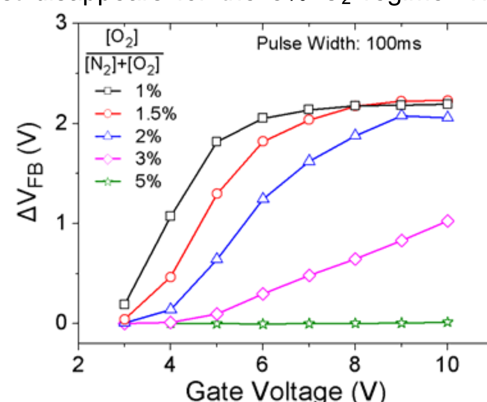

Fig. II.2.2: *Memory window characteristics obtained for MOS capacitors using 7nm-thick oxides implanted with 1keV Si to a dose of $2x10^{16}cm^{-2}$ and subsequently annealed in various oxidizing atmosphere.*

Task 2 Channel edge effects in shallow-trench-isolated nanocrystal memories

P. Dimitrakis and P. Normand

Within the framework of the EU project NEON, prototype LE-IBS-Si-nanocrystal memory devices were fabricated at STMicroelectronics (IT) on 8-inch wafers using a conventional process flow based on a 0.15μm Flash-EEPROM technology. The devices were isolated following a shallow-trench-isolation (STI) procedure. Capacitors and n-MOSFETs memory cells with gate lengths and widths ranging from 0.16 to 10 μm have been realized. Preliminary electrical investigations revealed that parasitic transistors (FET_P) formed at the channel edges affect drastically the device performance. The action of FET_P can be detected through a “subthreshold hump” in the transfer characteristics of the 10x10μm^2 and 0.9x0.6μm^2 (WxL) devices (see fig. II.2.3). Beyond this current hump, the device transcharacteristics correspond to that of the intrinsic transistor (FET_I) formed in the central part of the channel

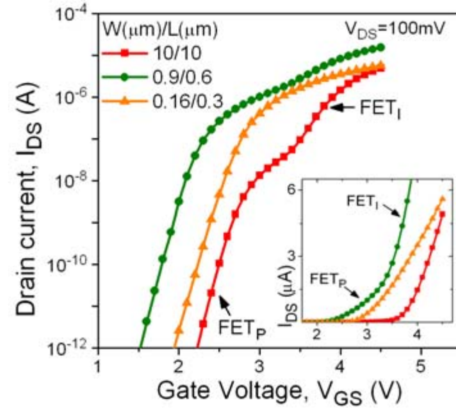

Fig. II.2.3: Typical I_{DS}-V_{GS} curves of ULE-IBS-NCMs with different channel

Major efforts have been devoted this year to understand and describe in a comprehensive way the effect of FET_P on the memory behavior of the devices. Memory testing revealed that the parasitic transistors can be programmed or erased but exhibit memory characteristics significantly different than that of FET_I. Typical results are shown in fig. II.2.4 where the memory windows are extracted from the transfer characteristics of the devices for different source-drain currents values. We also observed that the programming/erasing windows extracted from high I_{DS} in the case of 10μm/10μm devices are similar to the flat-band voltage shift curves obtained from large area (0.0096 cm^2) capacitors located on the same wafer than the transistors. This clearly indicates that any comparison in terms of memory behavior between capacitors and transistors will be misleading if the contribution of FET_P cannot be canceled. Finally, while no ‘subthreshold hump’ appears in the transfer characteristics of deep submicron (0.16x0.3μm^2) transistors, our investigations reveal that the parasitic transistors remain active and their operation dominates the memory behavior of the devices. The above findings stress out that the channel edge effects could constitute a technological issue towards the integration of nanocrystal floating-gate in conventional memory architecture.

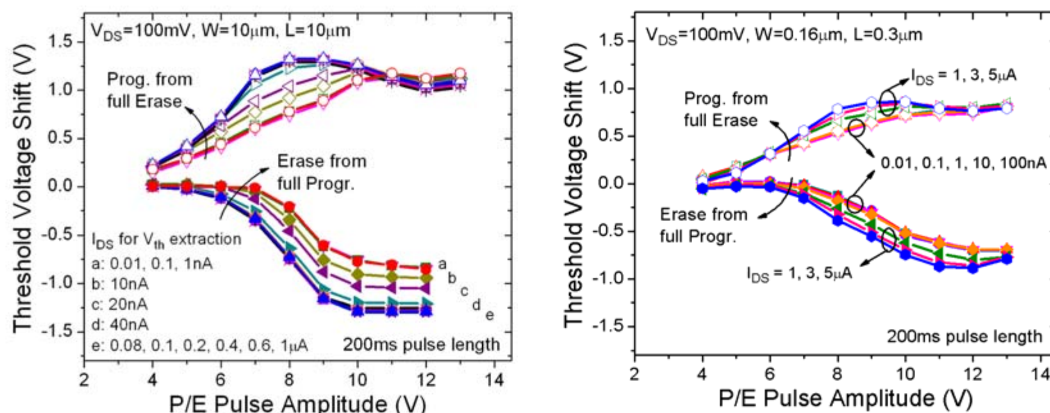

Fig. II.2.4: *Threshold voltage shift (ΔV_{th}) as a function of programming (P) and erasing (E) pulses for transistors with different channel areas: (left) W=10μm/L=10μm, (right) W=0.16μm/L=0.3μm. The P and E single pulses were applied from full E (-10V/200ms) and P (+8V/200ms) conditions, respectively, such as determined for 10μm/10μm FET_I and capacitors. ΔV_{th} has been calculated for different V_{th}-extraction I_{DS} values.*

Task 3 Hybrid SiGe/organic MOSFET with self-assembled Au-nps for memory applications

S. Kolliopoulou, P. Dimitrakis, D. Goustouridis, S. Chatzandroulis, P. Normand, D. Tsoukalas

Towards the realization of ultra-dense integrated circuits various technological approaches are currently explored. Three-dimensional (3-D) integration by using different 'memory' layers on the top of a silicon wafer where logic circuits are fabricated using conventional IC processing has been recently demonstrated. In this direction, our recent efforts have been devoted to the fabrication at low temperature of SiGe channel MOSFETs that allows further 3-D integration of multiple layers with functional devices [Kolliopoulou et al., Microelec. Eng., 2005]. The device fabrication procedure combines a low-temperature wafer-bonding process and the V-groove technique for channel definition. The latter is attractive since it can potentially lead to very short channel device architectures.

This year we concentrated our activities on the realization of low-temperature processed floating-gate type memory that combines the above V-groove SiGe MOSFET technology with deposition of charge storage nodes consisting of self-assembled Au nanoparticles (nps) and Langmuir-Blodgett (LB) films of organic insulators. A schematic diagram of the devices is shown in fig. II.2.5. Such structures were processed at a temperature lower than 400ºC. The 35-nm thick low-temperature oxide (LTO) of the gate stack was functionalized by surfactants containing amine groups. Au-nps were prepared separately and covered by specific organic ligands. Following functionalization, the SiGe sample was dipped into the Au-nps solution leading to the formation of a layer containing a high-density of well-ordered self-assembled Au-nps. Finally, 20 layers of Cadmium Arachidate were LB deposited to insulate the nanoparticles, and the gate electrode was then fabricated by Al evaporation and patterning.

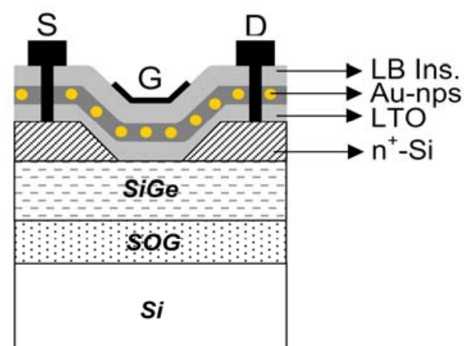

Fig. II.2.5: *A schematic cross-section of the hybrid organic-SiGe device with self-assembled Au-nps.*

The memory behavior of the devices was evaluated by applying positive and negative voltage pulses to the gate electrode while source and drain potentials were kept floating. For applied voltage pulses higher than ±12V, the threshold voltage of the devices is shifted with respect to the charges (electrons or holes) stored into (or extracted from) the nps. The I_{DS}-V_{GS} characteristics were monitored after gate pulsing in order to extract the threshold voltage. Such calculations were made according to the constant current method, and assuming a threshold drain-to-source current of 6.5×10^{-8}A. Memory windows as high as 7V for 1s programming time have been achieved (fig.II.2.6). It is important to note that due to the relatively thick LTO layer, the conduction properties of the LB insulator and the work functions of the used materials, electrons are extracted from the Au-nps to the gate electrode when applying positive gate pulses while pulses of opposite polarity cause electrons to move from the gate into the Au-nps.

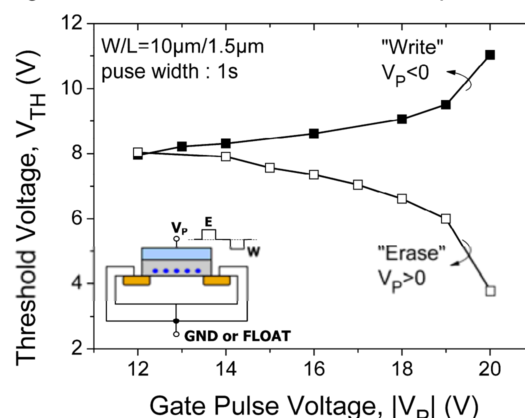

Fig. II.2.6: *Memory window characteristics of a hybrid organic/SiGe MOSFET with Au-nps.*

Task 4 Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride

V. Ioannou-Sougleridis, V. Vamvakas, P. Dimitrakis, D. Skarlatos, P. Normand

The use of thin tunnel SiO_2 layer (~2-3nm) in NCM technology allows high-speed operation at low voltages but addresses a critical issue for long retention times. If a thick oxide is used to enhance data retention, the advantage of high endurance and high speed at reasonable voltages is lost rapidly. Different alternatives have been suggested for improving the performance of NCMs operating in the direct tunneling regime. An interesting direction would be to combine the potential advantages (low-voltage and high-speed operation) of NCM technology with the advantages (long retention times, immunity to disturbance) of time-proven nitride-trap technology. Memory structures using SiO_2-Si_3N_4-SiO_2 (ONO) gate dielectric with nanocrystals embedded in the nitride layer are expected to gather together these advantages. While such an alternative, proposed by Motorola in 2002, has attracted a great deal of interest, much research and development is still required to establish a technology route that will be able to build a foothold in the NVM market.

In this direction, part of our research activities has been concentrated to the realization of Si-NC ONO structures where the Si-NCs are generated in the nitride layer by low-energy ion-beam-synthesis. SiO_2-Si_3N_4 structures were developed onto Si substrates and subsequently implanted at CEMES/CNRS with 1keV Si ions to a dose ranging from $5x10^{15}$ to $1.5x10^{16}$ cm^{-2}. The thickness of the oxide and nitride layers was 2.5nm and 6.5nm, respectively. After the steps of post-implantation annealing and SiO_2 deposition, gate electrodes were fabricated on part of the samples by Al evaporation and patterning. TEM examination of the 1keV /$1.5x10^{16}$ Si cm^{-2} implanted sample revealed the presence of Si-NCs into the nitride layer (see fig. II.2.7) together with a significant swelling of the SiO_2 and Si_3N_4 layers, respectively, 3.4 and 8.3nm in thickness. Preliminary investigations of the memory behavior of the above samples indicate enhanced charge storage (both electrons and holes) for the Si-NC ONO structures compared to the reference ONO samples (see fig. II.2.8). Typical memory windows attainable under pulse operation are shown in fig. II.2.9. In addition to our LE-IBS experiments, formation of Si-NC ONO structures by LPCVD of thin Si-rich-silicon nitride films and subsequent thermal annealing is currently examined in collaboration with project I.4.

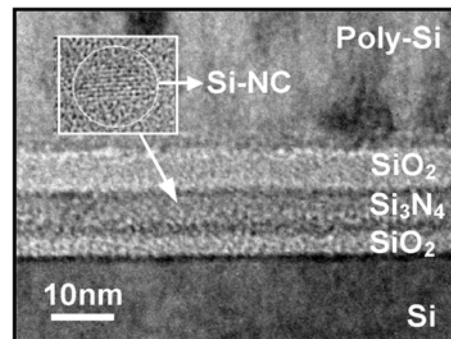

Fig. II.2.7: *Cross-sectional TEM picture of a Si-NC ONO structure. The NCs were generated in the nitride layer by LE-IBS (1keV / $1.5x10^{16}$ cm^{-2}).*

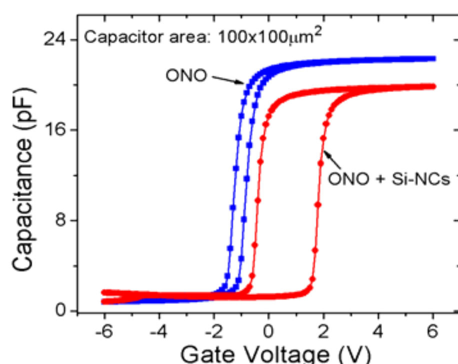

Fig. II.2.8: *Capacitance vs gate voltage round sweeps for ONO and Si-NC ONO dielectrics. The NCs were generated by LE-IBS (1keV / $1.5x10^{16}$ cm^{-2}).*

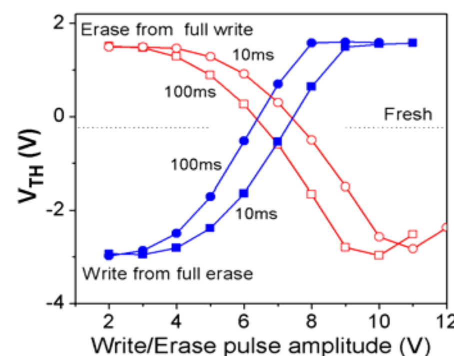

Fig. II.2.9: *Flat-band shifts after application of gate voltage pulses for Si-NC ONO dielectrics. The NCs were generated by LE-IBS (1keV / $1x10^{16}$ cm^{-2}).*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. "A Si/SiGe MOSFET utilizing low-temperature wafer bonding", S. Koliopoulou, P. Dimitrakis, D. Goustouridis, S. Chatzandroulis, P. Normand, D. Tsoukalas, H. Radamson, Microelectronic Engineering 78-79, 244 (2005).
2. "Recent advances in nanoparticle memories", D. Tsoukalas, P. Dimitrakis, S. Kolliopoulou, P. Normand, Mater. Sc. Eng. B 124-125, 93 (2005).
3. "Si nanocrystals by ultra-low energy ion implantation for non volatile memory applications", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, M. Carrada, G. Ben Assayag, A. Claverie, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, Mater. Sc. Eng. B 124-125, 499 (2005).
4. "Fabrication of nanocrystal memories by ultra low energy ion implantation", N. Cherkashin, C. Bonafos, H. Coffin, M. Carrada, S. Schamm, G. Ben Assayag, D. Chassaing, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, T. Muller, K. H. Heinig, A. Claverie, physica status solidi (c) 2,1907 (2005).
5. "Size and aerial density distributions of Ge nanocrystals in a SiO_2 layer produced by molecular beam epitaxy and rapid thermal processing", A. Kanjilal, J.L. Hansen, P. Gaiduk, A.N. Larsen, P. Normand, P. Dimitrakis, D. Tsoukalas, N. Cherkashin, A. Claverie, Appl. Phys. A 81, 363 (2005).
6. "Si nanocrystals by ultra-low-energy ion beam-synthesis for nonvolatile memory applications", C. Bonafos, H. Coffin, S. Schamm, N. Cherkashin, G. Ben Assayag, P. Dimitrakis, P. Normand, M. Carrada, V. Paillard, A. Claverie, Solid-State Electronics 49, 1734 (2005).

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. "Semiconductor nanocrystal floating-gate memory", P. Dimitrakis and P. Normand, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D5.1, pp. 203-216, 2005.
2. "Manipulation of 2D arrays of Si nanocrystals by ultra-low-energy ion beam-synthesis for nonvolatile memories applications", C. Bonafos, N. Cherkashin, M. Carrada, H. Coffin, G. Ben Assayag, S. Schamm, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, T. Muller, K.H. Heinig, A. Argawal, A. Claverie, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D5.2, pp. 217-222, 2005.
3. "Ge nanocrystals in MOS-memory structures produced by molecular-beam epitaxy and rapid-thermal processing", A. Nylandsted Larsen, A. Kanjilal, J. Lundsgaard Hansen, P. Gaiduk, P. Normand, P. Dimitrakis, D. Tsoukalas, N. Cherkashin, A. Claverie, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D6.2, pp. 263-267, 2005.
4. "Oxidation of Si nanocrystals fabricated by ultra-low energy ion implantation in thin SiO_2 layers", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, M. Respaud, G. Ben Assayag, P. Dimitrakis, P. Normand, M. Tencé, C. Colliex, A. Claverie, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D6.6, pp. 281-286, 2005.
5. "Gold Langmuir-Blodgett deposited nanoparticles for non-volatile memories", S. Kolliopoulou, D. Tsoukalas, P. Dimitrakis, P. Normand, S. Paul, C. Pearson, A. Molloy, M.C. Petty, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D6.7, pp. 287-292, 2005.
6. "Memory devices obtained by Si+ irradiation through poly-Si/SiO2 gate stack", P. Dimitrakis, P. Normand, E. Vontitseva, K.H. Stegemann, K.h. Heinig, and B. Schmidt, , in A. G. Nassiopoulou, N. Papanikolaou and C. Tsamis (Eds), Second Conference on Microelectronics, Microsystems and Nanotechnology, MMN-2004, Journal of Physics: Conference Series 10, pp. 7-10, 2005.
7. "Silicon nanocrystal memories by LPCVD of amorphous silicon, followed by solid phase crystallization and thermal oxidation", E Tsoi, P Normand, A G Nassiopoulou, V Ioannou-Sougleridis, A Salonidou and K Giannakopoulos, in A. G. Nassiopoulou, N. Papanikolaou and C. Tsamis (Eds), Second Conference on Microelectronics, Microsystems and Nanotechnology, MMN-2004, Journal of Physics: Conference Series 10, pp. 31-35, 2005.
8. "Field effect devices with metal nanoparticles integrated by Langmuir–Blodgett technique for non-volatile memory applications", S Kolliopoulou, D Tsoukalas, P Dimitrakis, P Normand, S Paul, C Pearson, A Molloy and M C Petty, in A. G. Nassiopoulou, N. Papanikolaou and C. Tsamis (Eds), Second Conference on Microelectronics, Microsystems and Nanotechnology, MMN-2004, Journal of Physics: Conference Series 10, pp. 57-60, 2005.

CONFERENCE PRESENTATIONS

1. "Control of Si nanocrystals fabricated by ultr-low energy ion implantation for non volatile memories", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, M. Carrada, G. Ben Assayag, A. Claverie, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, E-MRS 2005 Spring Meeting, Symposium D, Strasbourg, France, May 31 – June 3, 2005.
2. "Si nanocrystals by ultra-low-energy ion beam-synthesis for nonvolatile memory applications", C. Bonafos, H. Coffin, S. Schamm, M. Carrada, N. Cherkashin, G.B. Assayag, P. Dimittrakis, P. Normand, M. Perego, M. Fanciulli, Claverie, 1st International Conference on Memory Technology and Design (ICMTD), Giens, France, May 21-24, 2005.
3. "Metal nano-floating gate memory devices fabricated at low temperature", S. Koliopoulou, P. Dimitrakis, D. Goustouridis, P. Normand, C. Pearson, MC Petty, H. Radamson, D. Tsoukalas, International Conference on Micro- and Nano-Engineering, MNE 2005, Vienna, Austria, September 19-22, 2005. Best poster award – third price.

Ph. D. THESES

1. "Formation of semiconductor nanocrystals by ultra-low-energy ion-beam-synthesis and memory devices", E. Kapetanakis, National Technical University of Athens, April 2005, Supervisor: P. Normand
2. "Silicon nanoelectronic devices", S. Kolliopoulou, Aristotle University of Thessalonique, December 2005, Supervisor: D. Tsoukalas

INVITED TALKS

1. "Recent advances in nanoparticle memories", D. Tsoukalas, P. Dimitrakis, S. Kolliopoulou, P. Normand, E-MRS 2005 Spring Meeting, Symposium D, Strasbourg, France, May 31 – June 3, 2005.
2. "Nanocrystals and their application in nonvolatile memories", D. Tsoukalas, P. Dimitrakis, P. Normand, First International Workshop on Semiconductor Nanocrystals, SEMINANO 2005, Budapest, September 10-12, 2005.