Project III. 4

THIN FILM DEVICES for LARGE AREA ELECTRONICS

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Objectives

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors (TFTs) fabricated in such films. Such advanced TFTs are necessary for next generation large area electronics systems, which are now in the research and development phase. Specifically, the targets of the project are:

- Evaluation of device parameter (a) hot carrier and (b) irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polycrystalline silicon films utilizing sequential lateral solidification (SLS) techniques.
- Investigation of the influence of the polysilicon crystallization technique and the film thickness on TFT performance, defect densities and degradation for ELA technology optimization.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Investigation of effects of variations in TFT device structure and in the fabrication process on device performance and reliability.
- Assessment of material properties of advanced ELA polysilicon TFTs using optical measurements.
- Evaluation of bias stress-induced instabilities in solid phase crystallized (SPC) TFTs.

Funding

- PENED contract, project code 03ED550, 19/12/2005 – 18/12/2008.
- GSRT bilateral project Greece-Serbia, Polysilicon TFT reliability, 1/11/2004 – 30/4/2007.

RESEARCH RESULTS

A. Hot carrier stress investigation in ELA TFTs

TFT degradation under hot carrier stress (HCS) was investigated for devices fabricated in advanced 2-shot SLS ELA polysilicon films. TFTs with different channel widths and orientations relative to the grain boundary directions were compared. It was observed that the degradation of device parameters during HCS experiments was dependent on the channel width. Fig.III.4.1 shows the V_{th} evolution with stress time for a stress condition ($V_{GS,stress}$, $V_{DS,stress}$) = (3 V, 6 V), for X-directed TFTs. We observe an increase of ΔV_{th} for increasing stress time as a common behavior in all devices except the narrower ones, which exhibit an initial decrease and then an increase. The amplitude of the positive ΔV_{th} shift scales up with width. Narrower devices (W of 4 and 8 μm) demonstrate a less pronounced ΔV_{th} positive shift. The degradation behavior of Y-directed TFTs was in accordance with observations in X-directed devices. We also observed that devices with W = 16, 32 and 100 μm exhibit an initial increase in $G_{m,max}$ (transconductance “overshoot”) and then a reduction after a maximum $G_{m,max}$ value.

In order to investigate the width scaling of the additional energy source during hot-carrier experiments, we proposed that two width-dependent effects are involved, the floating body effect (FBE) and the self-heating effect (SHE). Concerning floating-body effects, we performed I_{DS}-V_{GS} electrical measurements with various drain voltages on wide and narrow devices, as shown in Fig.III.4.2. For higher drain voltages the parasitic bipolar transistor is activated giving rise to an abrupt drain current increase even at negative values of gate voltage (Fig.III.4.2), which indicates presence of FBEs. By performing various rates of drain voltage sweeps at V_{GS} = 3 V we could observe no significant increase or decrease of the drain current resulting from self-heating effects. However, it is possible that a temperature gradient may arise from the drain current, which is not observable in the output characteristics and at the same time may provide additional energy to the carriers; thus, the presence of SHEs is not excluded.

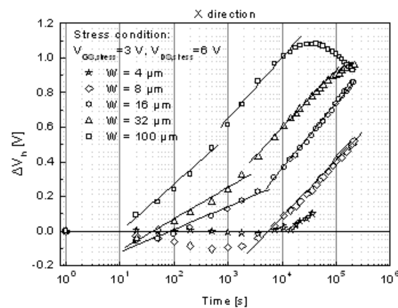


Fig. III.4.1: Threshold voltage variation versus stress time for X-directed polysilicon TFTs with various channel widths

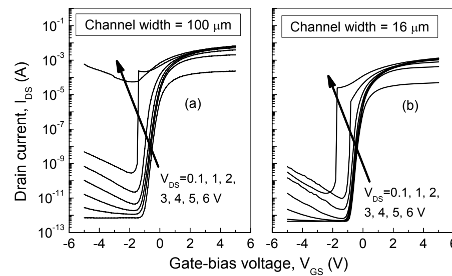


Fig. III.4.2: Transfer characteristics of polysilicon TFTs with channel widths of 100 μm and 16 μm for various drain-bias voltages.

Moreover, degradation phenomena due to HCS were investigated in double gate TFTs. We varied the HCS conditions at the front-gate channel by applying various back-gate voltages. We demonstrated that severe degradation phenomena may occur at the back interface depending on the back-gate voltage during stress. We observed that:

- Electrical stress with negative back-gate voltage enhances hot-hole injection in the back-gate oxide; hot-electron induced phenomena at the front polysilicon / SiO_2 interface also occur (Fig.III.4.3, 4).
- Electrical stress with positive back-gate voltage enhances hot-electron injection in the back-gate oxide; hot-hole injection occurs in the front oxide, combined with front interface state generation (Fig.III.4.5, 6).

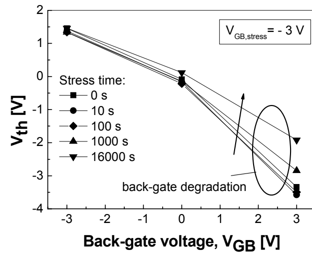


Fig. III.4.3: Threshold voltage as a function of back-gate voltage for various durations under stress condition with $V_{GB,stress}$= - 3 V.

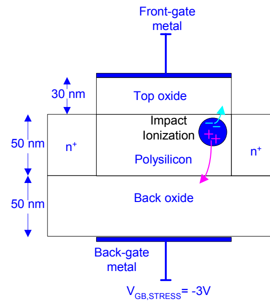


Fig. III.4.4: Schematic of top gate device and the degradation behavior for negative back-gate bias during stress.

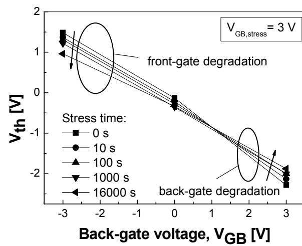


Fig. III.4.5: Threshold voltage as a function of back-gate voltage for various durations under stress condition with $V_{GB,stress}$= 3 V.

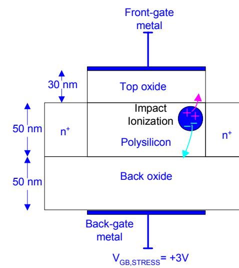


Fig. III.4.6: Schematic of top gate device and the degradation behavior for positive back-gate bias during stress.

In Table I we summarize the different degradation mechanisms for double gate devices for three stress regimes that were applied.

Stress $V_{GB,stress}$ [V]	Front interface degradation mechanisms	Back interface degradation mechanisms
- 3 V	State generation by hot-electrons at the polysilicon/SiO_2 interface and/or within the grain boundaries	Severe hot-hole injection and associated interface state generation
0 V	State generation by hot-electrons at the polysilicon/SiO_2 interface and/or within the grain boundaries	Mild hot-hole injection
+ 3 V	Severe hot-hole injection and interface state generation	Hot electron injection and associated interface-state generation

***Table I:** Degradation mechanisms for double gate ELA TFTs under hot carrier stress.*

B. Characterization of experimental ELA and IMEL-fabricated TFTs

Advanced variations of SLS ELA crystallization (termed 2^N-shot, M×N, Dot) have been applied for pilot fabrication of TFTs at Sharp; results from their characterization were presented in the 2006 report. This work was recently expanded to their reliability investigation, through the application of DC stress. We concluded that the different microstructural properties of the films resulted in different degradation behavior, both for the threshold voltage (Fig.III.4.7) and for the maximum transconductance (Fig.III.4.8).

Furthermore, we fabricated polysilicon TFTs at IMEL (with ELA crystallization at Sharp or SPC at IMEL) to probe the best technique for gate dielectric deposition and the effect of the crystallization technique on TFT performance and reliability. The mean performance parameters of all the fabricated TFTs can be seen in the following Table II.

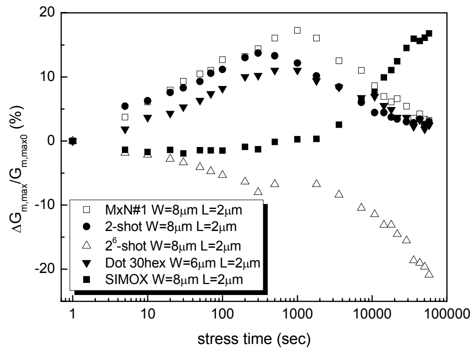


Fig. III.4.7: *Evolution of ΔV_{th} with stress time for differently crystallized poly-Si TFTs.*

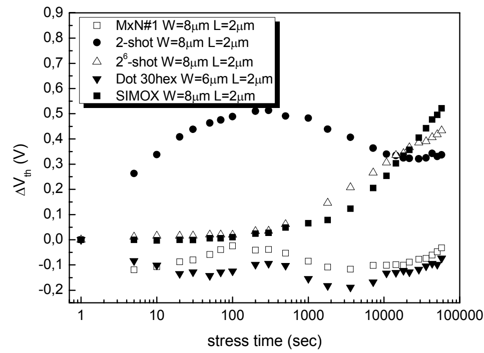


Fig. III.4.8: *Evolution of $\Delta G_{m,max}/G_{m,max0}$ with stress time for differently crystallized poly-Si TFTs.*

			BEFORE FGA	AFTER FGA	BEFORE FGA	AFTER FGA	BEFORE FGA	AFTER FGA	BEFORE FGA	AFTER FGA
SAMPLE	**POLY-SILICON**	**GATE DIELECTRIC**	**V_{th} (V)**		**μ (cm^2/V·sec)**		**D_{ts} ($eV^{-1}\cdot cm^{-2}$)**		**N_t (cm^{-3})**	
T1	D/S	PECVD SiO_2	1,32	0,37	51,12	91,07	$2{,}80\cdot10^{12}$	$8{,}97\cdot10^{11}$	$5{,}33\cdot10^{11}$	$2{,}27\cdot10^{11}$
T3	2-shot	PECVD SiO_2	2,11	1,00	32,02	65,99	$3{,}24\cdot10^{12}$	$1{,}25\cdot10^{12}$	$4{,}79\cdot10^{11}$	$2{,}40\cdot10^{11}$
T4	2-shot	TEOS SiO_2	0,79	0,72	82,44	104,33	$2{,}16\cdot10^{12}$	$1{,}07\cdot10^{12}$	$3{,}34\cdot10^{11}$	$2{,}33\cdot10^{11}$
T7	SPC	TEOS SiO_2	7,20	8,56	10,85	11,09	$7{,}81\cdot10^{12}$	$7{,}54\cdot10^{12}$	$9{,}23\cdot10^{11}$	$9{,}54\cdot10^{11}$

Table II: *Performance parameters of TFTs fabricated at IMEL.*

As far as reliability is concerned, we observed more severe degradation for the TFTs with 2-shot SLS ELA polysilicon (Fig.III.4.9), in comparison to ones with directional SLS ELA polysilicon, ascribed to the increased surface roughness of the film. Also, we observed different degradation mechanisms for TFTs with gate dielectric deposited with different techniques (Fig.III.4.10), ascribed to differences in the dielectric film quality.

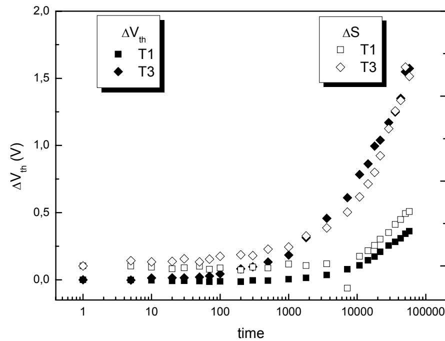


Fig. III.4.9: *Evolution of ΔV_{th} and ΔS with stress time for differently crystallized poly-Si TFTs.*

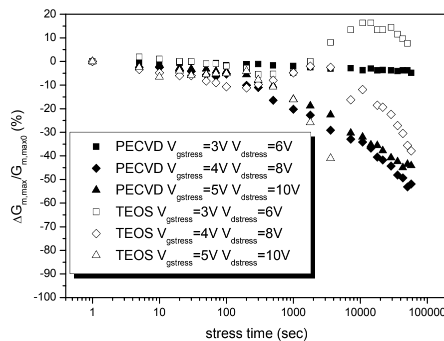


Fig. III.4.10: *Evolution of $\Delta G_{m,max}/G_{m,max0}$ with stress time for differently crystallized poly-Si TFTs.*

In an effort to investigate the use of a high-k material, HfO_2, as gate dielectric in TFT fabrication, we fabricated MOS capacitors with HfO_2 dielectric, to investigate the best HfO_2 sputter deposition and post-treatment conditions, and also determine which gate material would be suitable for this dielectric. Finally, we determined that the best performing MOS capacitors were the ones utilizing a thin SiO_2 oxide between the silicon and the HfO_2 film. We tried three different gate electrode materials, poly-Si, Al and W, and found that poly-Si is not a suitable material, since the capacitors exhibited high parasitic capacitances (Fig.III.4.11) and very low reliability. W gate samples performed acceptably (Fig.III.4.12), showing however some hysteresis, indicating charge trapping.

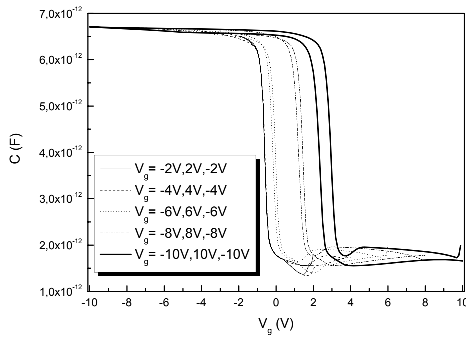


Fig. III.4.11: *Capacitance-Voltage characteristics for HfO_2 capacitors with poly-Si as gate electrode.*

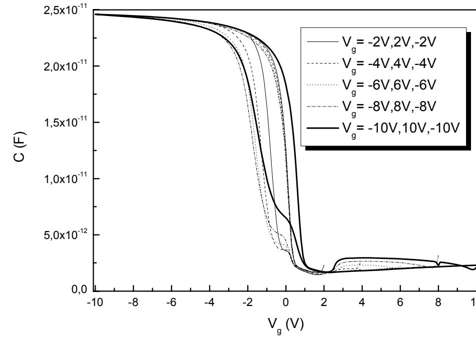


Fig. III.4.12: *Capacitance-Voltage characteristics for HfO_2 capacitors with W as gate electrode.*

C. Low temperature and transient current characterization

In the past year this research, carried out in collaboration with the University of Athens, was expanded in the investigation of the thermally activated mechanisms that determine the electrical properties of polysilicon TFTs (only a small part of the collaborative research at UoA is covered here). Temperature seems to have negligible effect on the ON regime, but significant influence below threshold, as indicated from the transfer characteristics in Fig.III.4.13; the OFF current and the subthreshold swing are thermally activated. The threshold voltage decreases with increasing temperature (Fig.III.4.14); in non-crystalline devices, the excitation of trapped carriers from band gap states into the conduction band plays a significant role, because the rise in temperature increases the free carrier density, leading to channel formation at lower gate voltages.

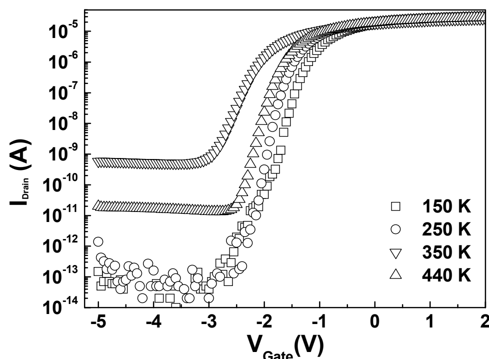


Fig. III.4.13: *Transfer characteristics of a TFT in a 100 nm thick polysilicon film at different*

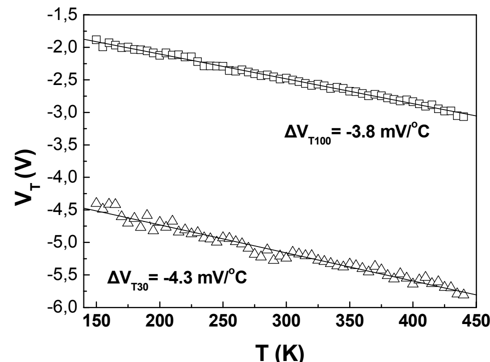
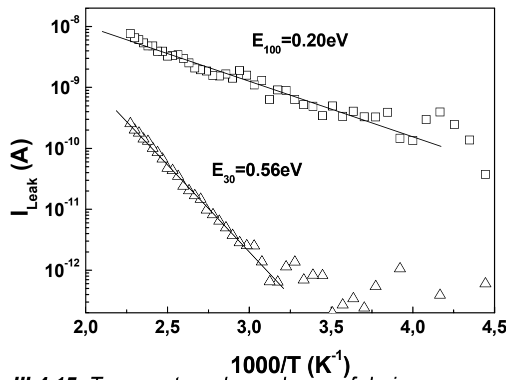


Fig. III.4.14: *Temperature dependence of threshold voltage for TFTs in 30 nm and 100 nm thick polysilicon films*

In polysilicon, carrier trapping, emission and thermal generation are determined by a continuous distribution of band gap states, which consists of band tails and deep traps. As the contribution of each state is thermally activated, the effective generation lifetime will also be, with effective activation energy E_A, which will depend on the distribution of the density of states. This allows the determination of E_A from the Arrhenius plot of the leakage current, in Fig.III.4.15; E_A was 0.20 eV and 0.56 eV for the 100 nm and 30 nm thick devices, respectively. The above values suggest that in thicker films the generation takes place mainly through deeper states, while in thinner films the contribution of tail states becomes significant. As tail states are mainly introduced due to the lack of periodicity in the crystal potential, by the presence of grain boundaries, a large density of tail states is expected in thinner SLS polysilicon films where the grains are smaller.



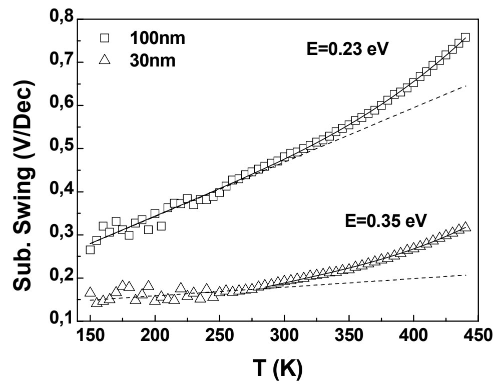


Fig. III.4.15: *Temperature dependence of drain leakage current for TFTs in 30 nm and 100 nm thick films.*

Fig. III.4.16: *Exponential terms obtained in the subthreshold swing increase with temperature for 30 nm and 100 nm TFTs.*

In TFTs the subthreshold swing is temperature dependent primarily due to the increase in the intrinsic carrier concentration, while the Fermi level and mobility variations are also involved. In bulk MOSFETs, a linear swing increase with increasing temperature is expected due to the diffusion nature of the current. In polysilicon TFTs the generation of carriers takes place through grain boundary trap states. In principle, the generation mechanism in the depletion layer is the same with the one for the leakage current. Therefore, the activation energies, derived from the subthreshold swing, must have similar values and follow the same trend, with respect to the film thickness, with the ones obtained from the OFF state leakage current. Comparing (Fig.III.4.16) the values of the activation energies we find that for TFTs in 100 nm films the activation energies are practically the same. In contrast, in the case of 30 nm thick film devices the activation energies are different; lower values are obtained from the temperature dependence of the subthreshold swing. This difference may be attributed to the effect of coupling of the front and back interfaces, which is directly affected by the inefficient screening from body defects, as the electron mean free path is estimated in the range of 5–30 nm that is close to the film thickness. Such a situation seems not to occur for the 100 nm devices, where the polysilicon film thickness is much larger than the electron mean free path.
The temperature dependence of TFT parameters (leakage current, subthreshold swing) was thus found to stem from the same thermally activated carrier generation mechanism through grain boundary trap states, which determines device operation; deeper states contribute more to the generation in 100 nm films than in 30 nm ones. The leakage current, the exponential increase of the subthreshold swing and the switch-ON overshoot transient current amplitude exhibit the same temperature onset; the threshold temperature of those thermally activated processes is found to be thickness dependent, indicating the varying contribution of trap states. The dependence of thermally activated mechanisms, which are strongly related to material properties and which shape the electrical characteristics, on film thickness suggests that TFT operation is strongly related to the polysilicon film properties, in particular to the contribution of trap states.

D. Irradiation investigation

The γ-irradiation induced degradation of SLS ELA TFTs has also been studied, in collaboration with the University of Nis. During 2007, while the effect of polysilicon film thickness was further explored, the research was expanded to investigation of the effect of device direction relative to the preferred direction of directional SLS ELA polysilicon films, as well as to the assessment of the grain boundary trap state density. Fig.III.4.17 shows the threshold voltage shift after irradiations of 100 Gy and 500 Gy, for various film thicknesses; TFTs fabricated in intermediate thickness films seem to have higher immunity to irradiation. The V_{th} shift strongly depends on the gate voltage applied during irradiation for TFTs in 30 nm and 100 nm polysilicon films, while for TFTs in 50 nm films the influence of this gate bias is no so pronounced, especially in devices oriented with the current flow orthogonal to the elongated grains.

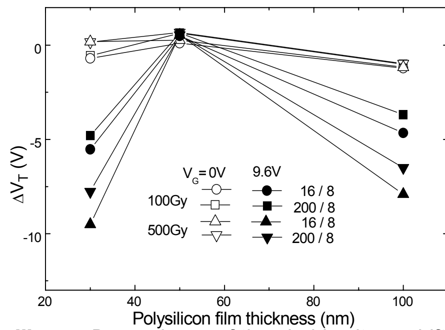


Fig. III.4.17: *Dependence of threshold voltage shift on poly-Si film thickness for doses of 100 & 500 Gy.*

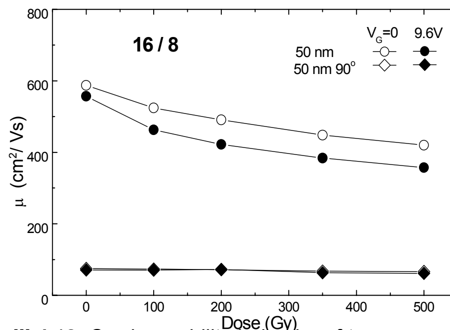


Fig. III.4.18: *Carrier mobility behavior of two groups of irradiated TFTs having different direction of current flow.*

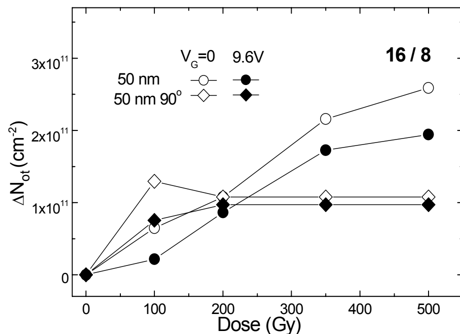


Fig.III.4.19:*Oxide trapped charge density for irradiated TFTs having different direction of current flow.*

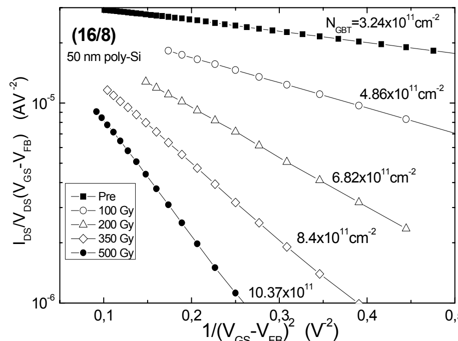


Fig. III.4.20:*Typical graph for grain boundary trap-state density extraction of stressed TFT devices.*

Fig 18 shows the electron mobility for TFTs in 50 nm films oriented in parallel or perpendicularly (90º) to the preferred grain direction. The weak dependence of mobility on irradiation dose, as well as on gate bias during irradiation, which is observed, could be attributed to domination of scattering mechanisms and trapping at grain boundaries over scattering on charged interface defects. This conclusion can be further supported from the comparison of the mobility in devices having current flow direction orthogonal to the grain boundaries; in these TFTs the mobility is not only low and independent of γ-irradiation dose, but also almost independent of applied gate bias during irradiation.

TFTs in 50 nm polysilicon films exhibit a small irradiation-induced degradation of the oxide trapped charge density (N_{ot}), which is significantly smaller in devices having orientation at 90° with respect to the preferred grain direction, as shown in Fig.III.4.19; moreover, for these devices there is almost no effect of gate bias application during irradiation. Besides the grain size, the quality of polysilicon films is also defined by trap states at grain boundaries, which influence the mobility at higher gate voltages. Using the procedure described by Proano et al (IEEE TED-36, 1915, 1989), a modification of the Levinson method), the density of grain-boundary trap states (N_{GBT}) in virgin and stressed devices can be determined from the slopes of the straight lines of the plots shown in Fig.III.4.20. As can be seen, virgin TFTs have N_{GBT} = 3-5x10^{11} cm^{-2}, while γ-irradiation generates new traps at grain-boundaries, degrading the device parameters. Fig.III.4.21 shows the shift in N_{GBT} against the irradiation dose for TFTs (parallel to grains) in 30, 50 or 100 nm films. TFTs in 100 nm films are much less resistant to irradiation when a gate bias is applied for duration of it. Fig.III.4.22 shows the N_{GBT} against irradiation dose for TFTs in 50 nm films oriented in parallel or vertically to the elongated grains; the effect of an applied gate bias during irradiation is not significant here. While the difference is small, the vertically oriented devices are more resistant to γ-irradiation.

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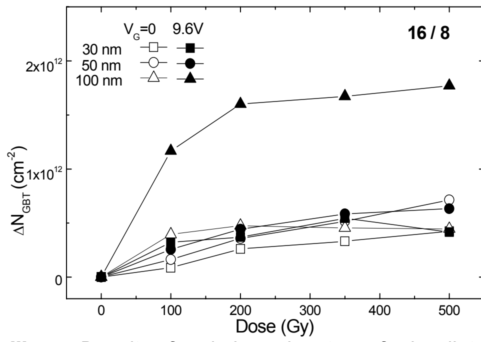

Fig. III.4.21:*Density of grain boundary traps for irradiated TFTs having different thickness of polysilicon films.*

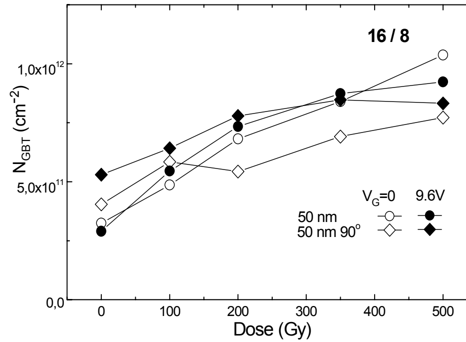

Fig. III.4.22: *Density of grain boundary traps for irradiated TFTs having different direction of current flow.*

E. Material / optical characterization

An optical characterization of three differently crystallized SLS ELA polysilicon films was performed. TFTs fabricated in these three types of films (directional, 2-shot and 2^6-shot) have also been electrically characterized. The transmission spectra of the polysilicon films were obtained (Fig.III.4.23). We fitted these spectra with a software developed here, utilizing the Tauc-Lorentz model for the refractive index of the material, in order to extract the real (Fig.III.4.24) and the imaginary part of the refractive index of the films. This way, structural differences between the various polysilicon films could be probed. Through the optical parameters extracted, a correlation between structural and electrical characteristics will be attempted.

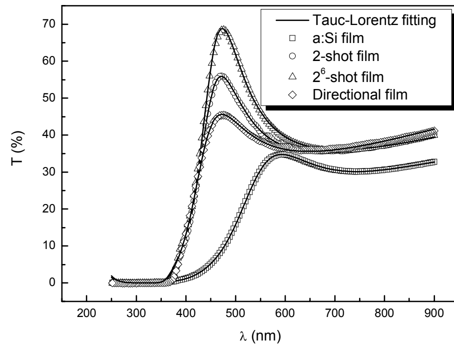

Fig. III.4.23: *Transmission spectra of the SLS ELA poly-Si films and application of Tauc-Lorentz model.*

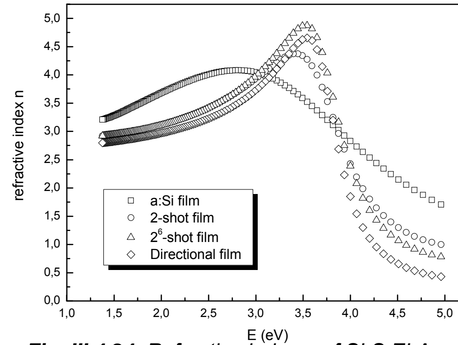

Fig. III.4.24: *Refractive index n of SLS ELA poly-Si films, as obtained by the Tauc-Lorentz model.*

PROJECT OUTPUT in 2007

Publications in International Journals and Reviews

1. "An experimental study of the thermally activated processes in polycrystalline silicon thin film transistors", Michalas, L., M. Exarchos, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, Microelectronics Reliability, 47 (12), 2058, December 2007.
2. "Influence of polysilicon film thickness on radiation response of advanced excimer laser annealed polycrystalline silicon thin film transistors", Davidovic, V., D.N. Kouvatsos, N. Stojadinovic and A.T. Voutsas, Microelectronics Reliability 47 (9-11), 1841, September-November 2007.
3. "Degradation of double-gate polycrystalline silicon TFTs due to hot carrier stress", Farmakis, F.V., G.P. Kontogiannopoulos, D.N. Kouvatsos and A.T. Voutsas, Microelectronics Reliability 47 (9-11), 1434, September-November 2007.
4. "Performance and reliability of SLS ELA polysilicon TFTs fabricated with novel crystallization techniques", Moschou, D.C., M.A. Exarchos, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, Microelectronics Reliability 47 (9-11), 1378, September-November 2007.
5. "Front and Back Channel Properties of Asymmetrical Double-Gate Polysilicon TFTs", Farmakis, F.V., D.N. Kouvatsos, A.T. Voutsas, D.C. Moschou, G.P. Kontogiannopoulos and G.J. Papaioannou, Journal of the Electrochemical Society 154 (10), H910, October 2007.
6. "Nickel nanoparticle deposition at room temperature for memory applications", Verelli, E., D. Tsoukalas, K. Giannakopoulos, D. Kouvatsos, P. Normand and D.E. Ioannou, Microelectronic Engineering, 84 (9-10), 1994, September-October 2007.
7. "Device degradation behavior and polysilicon film morphology of TFTs fabricated using advanced excimer laser lateral solidification techniques", Kouvatsos, D.N., A.T. Voutsas, L. Michalas, F. Farmakis and G.J. Papaioannou, Thin Solid Films 515 (19), 7413, July 2007.
8. "Characterization of double gate TFTs fabricated in advanced SLS ELA polycrystalline silicon films", Kouvatsos, D.N., F.V. Farmakis, D.C. Moschou, G.P. Kontogiannopoulos, G.J. Papaioannou and A.T. Voutsas, Solid State Electronics 51 (6), 936, June 2007.

Publications in Conference Proceedings

1. "The impact of gate oxide polarization on drain current transient behavior of advanced excimer laser crystallized polysilicon thin film transistors", Exarchos, M.A., L. Michalas, G.J. Papaioannou, D.N. Kouvatsos, and A.T. Voutsas, Proceedings of the 3rd International Thin Film Transistors Conference (ITC '07) / 2007 Society for Information Display Europe Chapter Meeting, p. 196, Rome, Italy, 2007.
2. "Characterization of advanced directional SLS ELA polysilicon TFTs – Dependence of device parameters on orientation and geometry", Moschou, D.C., D.N. Kouvatsos, F.V. Farmakis and A.T. Voutsas, Proceedings of the 3rd International Thin Film Transistors Conference (ITC '07) / 2007 Society for Information Display Europe Chapter Meeting, p. 192, Rome, Italy, January 2007.
3. "Investigation of the Undershoot Effect in Polycrystalline Silicon Thin Film Transistors", Michalas, L., G.J. Papaioannou, D.N. Kouvatsos, and A.T. Voutsas, Proceedings of the 3rd International Thin Film Transistors Conference (ITC '07) / 2007 Society for Information Display Europe Chapter Meeting, p. 116, Rome, Italy, January 2007.
4. "Hot carrier stress induced degradation of SLS ELA polysilicon TFTs – Effects of gate width variation and device orientation", Kontogiannopoulos, G.P., F.V. Farmakis, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, Proceedings of the 3rd International Thin Film Transistors Conference (ITC '07) / 2007 Society for Information Display Europe Chapter Meeting, p. 100, Rome, Italy, January 2007.

International Conference Presentations

1. "The effect of crystallization technology and gate insulator deposition method on the performance and reliability of polysilicon TFTs", Moschou, D.C., G.P. Kontogiannopoulos, D.N. Kouvatsos and A.T. Voutsas, 3rd International Conference on Micro- and Nanoelectronics, Nanotechnology and MEMS (MicroNano 2007), Athens, Greece, November 2007.
2. "Performance of Thin-Film Transistors fabricated by Sequential Lateral Solidification crystallization techniques", Exarchos, M.A., D.C. Moschou, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, 3rd International Conference on Micro- and Nanoelectronics, Nanotechnology and MEMS (MicroNano 2007), Athens, Greece, November 2007.
3. "Investigation of top gate electrode variations for high-k gate dielectric MOS capacitors", Moschou, D.C., E. Verelli, D.N. Kouvatsos, P. Normand, D. Tsoukalas, A. Speliotis, P. Bayiati and D Niarchos, 3rd International Conference on Micro- and Nanoelectronics, Nanotechnology and MEMS (MicroNano 2007), Athens, Greece, November 2007.
4. "An Experimental Study of Band Gap States Electrical Properties in Poly-Si TFTs by the Analysis of the Transient Currents", Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, 3rd International Conference on Micro- and Nanoelectronics, Nanotechnology and MEMS (MicroNano 2007), Athens, Greece, November 2007.
5. "Degradation of double gate polycrystalline silicon TFTs due to hot carrier stress", Farmakis, F.V. G.P. Kontogiannopoulos, D.N. Kouvatsos and A.T.Voutsas, 18th European Symposium - Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2007), Arcachon, France, October 2007.

6. “Influence of polysilicon film thickness on radiation response of advanced excimer laser annealed polycrystalline silicon thin film transistors”, Davidović, V., D.N. Kouvatsos, N. Stojadinović, A.T. Voutsas, 18th European Symposium - Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2007), Arcachon, France, October 2007.
7. “Performance and reliability of SLS ELA polysilicon TFTs fabricated with novel crystallization techniques”, Moschou, D. C., M. A. Exarchos, D. N. Kouvatsos, G. J. Papaioannou and A. T. Voutsas, 18th European Symposium - Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2007), Arcachon, France, October 2007.
8. “Characterization of thin film transistors fabricated on different sequential lateral solidified poly-silicon substrates”, Michalas, L., G.J. Papaioannou, D.N. Kouvatsos, F.V. Farmakis and A.T. Voutsas, 33rd International Conference on Micro- and Nano-Engineering (MNE 2007), Copenhagen, Denmark, 2007
9. “A novel SLS ELA crystallization process and its effects on polysilicon film defectivity and TFT performance”, Moschou, D. C., M. A. Exarchos, D. N. Kouvatsos, G. J. Papaioannou and A. T. Voutsas, 33rd International Conference on Micro- and Nano-Engineering (MNE 2007), Copenhagen, Denmark, September 2007.
10. “Nickel nanoparticle deposition at room temperature for memory applications”, Verelli, E., D. Tsoukalas, K. Giannakopoulos, D. Kouvatsos, P. Normand and D.E. Ioannou, 15th bi-annual Conference – Insulating Films on Semiconductors (INFOS 2007), Athens, Greece, June 2007.

Conference Participation

1. 3rd International Thin Film Transistors Conference (ITC ’07) / 2007 Society for Information Display Europe Chapter Meeting, Rome, Italy, January 2007.
2. 15th bi-annual Conference – Insulating Films on Semiconductors (INFOS 2007), Athens, Greece, 2007.
3. 33rd International Conference on Micro- and Nano-Engineering (MNE 2007), Copenhagen, Denmark, September 2007.
4. 18th European Symposium - Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2007), Arcachon, France, October 2007.
5. 3rd International Conference on Micro- and Nanoelectronics, Nanotechnology and MEMS (MicroNano 2007), Athens, Greece, November 2007.
6. 23rd Panhellenic Conference for Solid State Physics and Materials Science, Athens, Greece, September 2007 (5 presentations).

Organization of Conferences, Workshops and Project meetings

1. Member of the Technical Programme Subcommittee of the 18th European Symposium - Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2007), Arcachon, France, October 2007.
2. Reviewer – Member of the Technical Programme Subcommittee of the 26th International IEEE Conference on Microelectronics (MIEL 2008) (Nis, Serbia & Montenegro, May 2008).