Project III. 5

CIRCUITS & DEVICES FOR OPTOELECTRONIC INTERCONNECTIONS

Project Leader: G. Halkias

Other Key Researchers: S. G. Katsafouros
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Objectives

The main objective of the activity is the development of the technologies for future high-density and high-speed optoelectronic interconnections. In the context of this objective the research targets of optoelectronic device modeling and simulation, implementation of optoelectronic technology in spacecraft environment as well as packaging in terms of photonic link integration above CMOS integrated circuits have been identified and pursued.

Funding

- EU- IST PICMOS - Contract No 002131, **"**Photonic Interconnet Layer on CMOS by Wafer-Scale Integration", Duration: 1/1/2004-31/3/2007

RESEARCH RESULTS

A. Development of a model for simulating Vertical Cavity Surface Emitting Lasers (VCSELs)

A compact non-linear circuit model for the input of packaged high-speed VCSELs is presented. The model includes the thermal effects as well as the parasitics, due to the various levels of the packaging hierarchy, to ensure a realistic representation of the input of the VCSELs. The values of the model parameters are extracted from dc current-light-voltage characteristics and S_{11} vector measurements using a two-step parameter extraction procedure. Extraction of the model parameters and comparison between measured and simulated results have been performed for two different commercially available VCSELs operating at 2.5Gb/s. The achieved agreement between the measured and simulated results is very satisfactory for the dc as well for the S_{11} curves in the frequency range from 3MHz to 3GHz.

B. Heterogeneous integration of optical interconnects onto CMOS ICs

The employment of a photonic layer above CMOS integrated circuits (ICs) has been proposed as an alternative solution for the global interconnection regime. Photonic dies with fully integrated optical paths, sources and detectors coupled to waveguides, are bonded onto a CMOS integrated circuit (IC) using a metallic bonding technique. The proposed approach utilizes a thin multilayer structure of the 80Au-20Sn eutectic alloy along with a thin starting layer of rare earth Gd and contains versatile structures for passive alignment. Its main advantage is the fact that it accomplishes mechanical bonding and electrical connectivity in a single step. The proposed approach resembles the flip-chip approach, but the solder volume and size are considerably lower making it appropriate for high-density integration. Pattern uniformity, limited alloy spreading and contact resistance in the mΩ range across a 4-inch wafer has been verified. Figure 1 below shows on top a portion of a patterned 4in wafer where convex structures are formed to match with the corresponding concave structures patterned on the dies and below IR images of bonded dies. It becomes clear that the goal of alignment has been achieved as also revealed by electrical measurements of the test structures shown in figure 2. This project is executed in collaboration with IMEC, Belgium, ST, CEA, CNRS-FMNT, France, and TUE, Holland, in the framework of the European project PICMOS.

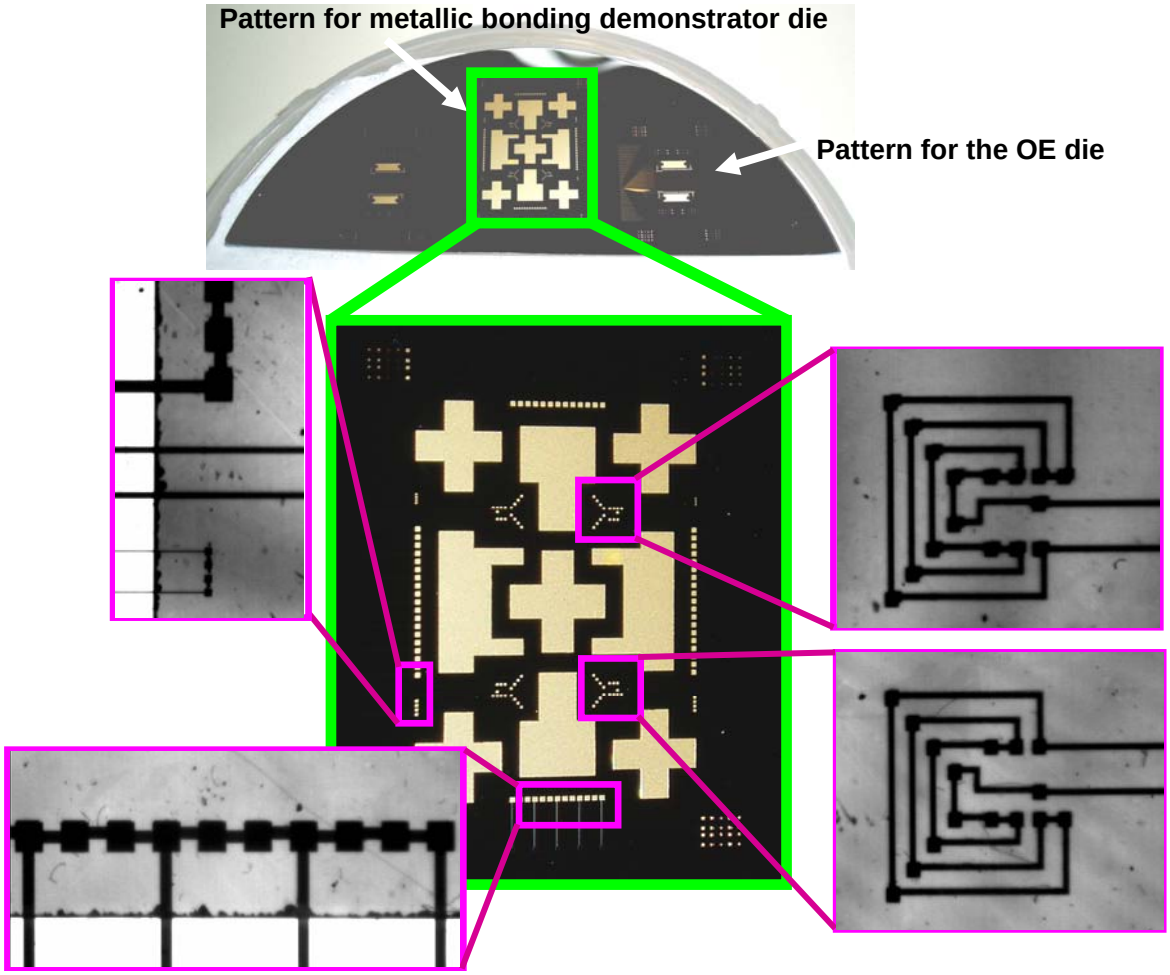

Fig. III.5.1: Wafer and die photographs and IR images of bonded structures

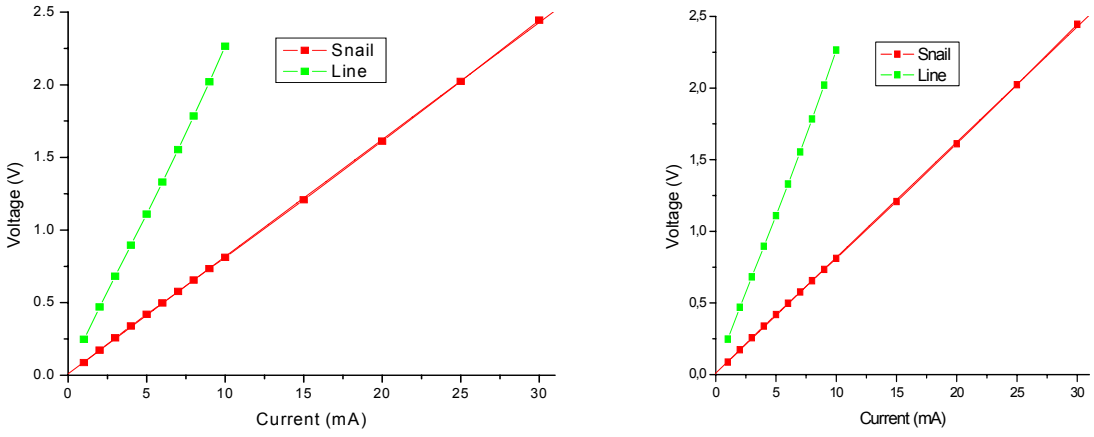

Fig. III.5.2: Electrical measurements of bonded test structures.

PROJECT OUTPUT IN 2007

PUBLICATIONS in REFERREED JOURNALS

1. "Input and intrinsic device modeling of VCSELs", K. Minoglou, G. Halkias, E. D. Kyriakis-Bitzaros, D. Syvridis, Journal of Computational Electronics, Springer Science, Vol. 6, 2007, pp.309–312

CONFERENCE PRESENTATIONS

1. "VCSEL device modeling and parameter extraction technique", K.Minoglou, G.Halkias, E.D.Kyriakis-Bitzaros, D.Syvridis, A.Arapogianni, IEEE 14th ICECS 2007,Marrakesh,Morocco, 11-14 Dec. 2007, pp. 14-17
2. "High density integrated optoelectronic circuits for high speed photonic Microsystems", K.Minoglou, E.D.Kyriakis-Bitzaros, S.G. Katsafouros, G.Halkias, A.Arapogianni, and D.Syvridis, PRIME 2007, Bordeaux, France, pp 57-60.

PhD Thesis

1. "High density optoelectronic integrated circuits for high speed photonic microsystems", K. Minoglou, Department of Informatics and Telecommunications, University of Athens, March 2007.

PAPER AWARDS

1. Paper C2 was awarded the "Bronze Leaf" (third prize)