PROJECT II.1 and III.1

NANOSTRUCTURES FOR NANOELECTRONICS, PHOTONICS AND SENSORS

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Research orientation:

- Semiconductor nanostructures: Growth, characterization (electrical, optical, structural), applications
- Porous Si technology for sensors
- Porous anodic alumina thin films for masking and templating applications
- RF isolation by porous silicon micro-plates on a silicon substrate
- Self-assembly of dots and nanowires
- Theory (Ballistic transport in nanostructures, Surface plasmons in thin metallic films, classical molecular dynamics and nanoscale heat transport)

a) Nanostructure growth, characterization and applications

The activity on semiconductor nanostructures started at IMEL at the early nineties and it was conducted within different EU projects, in collaboration with other European groups (Esprit-EOLIS, contract No 7228 (1992-95) Esprit FET SMILE contract No 28741 (1998-2000), IST FORUM FIB contract No 29573 (2001-2004), IST-FP6 NoE SINANO contract No 506844 etc). Worldwide original results were produced, including fabrication of light emitting silicon nanopillars by lithography and anisotropic etching and investigation of their optical and electrical properties, growth of Si nanocrystal superlattices by LPCVD and high temperature oxidation/annealing, with interesting optical properties, fabrication and characterization of LEDs based on Si nanopillars and nanodots, fabrication of Si and Ge nanocrystals embedded in SiO_2 and fabrication and investigation of the corresponding memory structure.

The present focus of research is on self-assembly and ordering of nanostructures and their different applications in nanoelectronics, photonics and sensors. Porous alumina template and masking technology are also developed. Porous alumina ultra-thin films are grown on silicon by electrochemistry. By appropriately choosing the electrochemical conditions used, pore size and density are monitored. Through-pore silicon nanostucturing follows the pore size and density. Arrays of SiO_2 nanodots on Si are fabricated and characterized. Dot size varies from few nm up to few hundreds of nm.

Another technology under development is the growth of ultra thin porous silicon films by electrochemical dissolution of silicon in the transition regime between porosification and

electropolishing. Under appropriate conditions, the obtained films are amorphous with embedded Si nanocrystals of various sizes. Under other conditions, the films are nanocrystalline. Their properties are investigated in view of different applications in nanoelectronics and photovoltaics.
The theoretical group focuses on the investigation of ballistic transport in nanostructures,surface plasmons in thin metallic films, classical molecular dynamics and nanoscale heat transport.

b) Porous silicon technology for sensors

An important effort has been devoted the last years within the group in developing materials and enabling technologies for application in sensors. One such material platform with important potential for applications in different sensor devices, microfluidics, lab-on-chip, integration of passives on silicon etc, is porous silicon technology.

Either mesoporous or nanoporous/macroporous silicon are grown. Mesoporous silicon is nanostructured and appropriate for use as micro-plate for local thermal or electrical (dc, RF) isolation on a silicon substrate. Nanoporous Si is also used in the above, after further treatment. Macroporous silicon is developed for use in via technology, in device cooling and in particle filtering.

Different technologies based on porous silicon are available at IMEL, including:

- Proprietary micromachining techniques based on the use of porous silicon as a sacrificial layer for the fabrication of free standing membranes, bridges and cantilevers on a silicon substrate
- Technologies using porous silicon for local thermal or for RF isolation on a silicon wafer, or using porous silicon as a matrix for the deposition of catalytic materials for use in chemical sensors

c) RF isolation by porous silicon micro-plates on a silicon substrate

The overall objective of this research is:

- to explore and extend porous silicon technology into the domain of CMOS-compatible integrated RF components and
- to improve the performance of currently integrated analog CMOS components by above technology, and related optimization of design methodologies.

EXAMPLES OF RESEARCH RESULTS IN 2007

A. Successive Layer Charging of Si Nanocrystals in a Double-Nanocrystal-Layer Structure within SiO_2

M. Theodoropoulou, and A. G. Nassiopoulou

Layers of silicon nanocrystals embedded in SiO_2 were fabricated by low-pressure chemical vapor deposition (LPCVD) of α-Si, followed by high temperature thermal oxidation and annealing. The thickness of the amorphous layer as well as the oxidation time are chosen to give the desired thickness of the nanocrystal layer and the top oxide.
By using the above process, double layers of silicon nanocrystals were fabricated within the gate dielectric of a MOS memory structure (Fig.1). This structure is expected to open important new possibilities in multiple bit operation memories.
To investigate the charging properties of the silicon nanocrystal layers, capacitance-voltage (*C-V*) measurements were performed at 1MHz at room temperature, by applying positive and negative gate pulses of different height and width on the gate. Fig. 2 shows *C-V* curves of a fresh capacitor (before the application of a gate pulse) and the same capacitor after application of positive or negative gate pulses. When a positive or a negative gate pulse is applied, a positive or negative shift in the flatband voltage of the MIS structure is obtained, indicative of charging the silicon nanocrystal layers with electrons (holes) respectively from the Si substrate. Fig. 3 shows the flatband voltage shift ΔV_{FB} as a function of the applied positive or negative gate pulse height. We clearly distinguish distinct steps in the curves, that

correspond to the successive charging of the first and second nanocrystal layer respectively. Full charging of the first layer occurred at ±3V (shift in flat band voltage: ± 0.5 V), while of the second layer at end voltages of ±8V (positive shift: 2.1V, negative shift: -2.8V). Retention measurements show improved charge retention compared to a single-dot layer structure.
The above results are very promising for application of the structure in multi-bit memory devices.

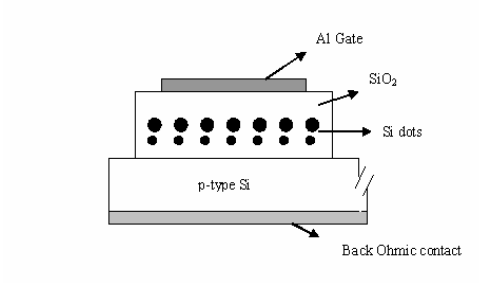


Fig.1. *2-NC-layer MIS structure*

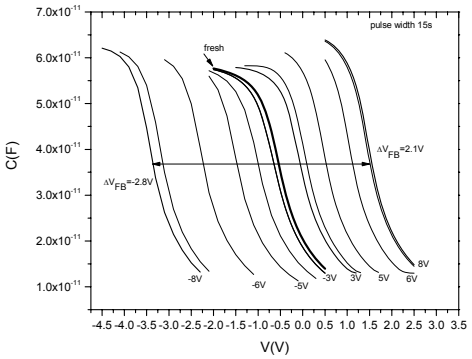


Fig.2. *Capacitance-Voltage (C-V) curves from a structure with embedded NCs showing successive charging by electrons (positive shift) or holes (negative shift), injected from the substrate under pulse application*

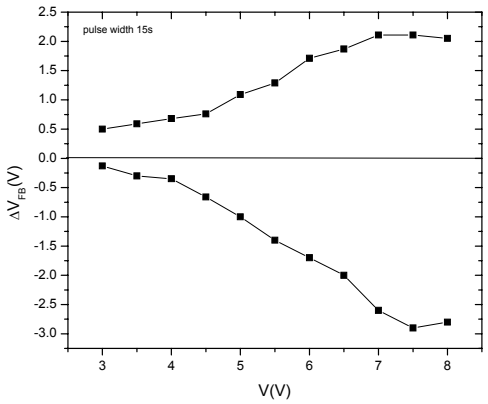


Fig.3. *ΔV_{FB} as a function of voltage for the double-NC-layer structure*

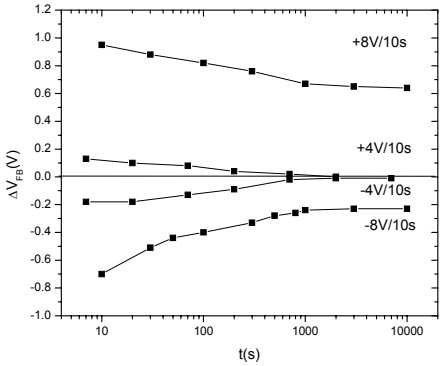


Fig.4. *Charge retention as a function of time of the first NC layer (charged by pulses at ±4V/10s pulse) and second NC layer, charged by pulses at ±8V/10s*

B. Investigation of the structure, topography, chemical composition and optical properties of thin anodic silicon films, grown using short monopulses of current.

S. Gardelis and A.G. Nassiopoulou

In collaboration with N. Frangis from the Physics Depart. of Aristotle Univ. of Thessal. and with S. Kennou of the Depart. of Chemical Engineering, Univ. of Patras and FORTH/ICE-HT[3] 26504 Patras

Very thin (almost 2-dimensional (2-D)) Si nanocrystal layers were grown by anodization of bulk crystalline Si in the transition regime between porous formation and electropolishing. The films were investigated for their structure, morphology, chemical composition and light emitting properties. Two types of films were investigated. Type A was fabricated using low HF (hydrofluoric acid) concentration electrolyte and type B using high HF concentration electrolyte. Both films were grown using the same current density. Atomic force microscopy (AFM) images obtained from the two types of film showed significant difference in their morphology. Both showed a grain-like surface topography (Fig. 1a). Type A was rougher, than type B, showing an average microroughness of about 10 nm, whereas type B showed a much smoother surface morphology with an average microroughness of 1.5- 2 nm. From cross-sectional bright field Transmission Electron Microscopy (TEM) images, the thickness of

film A was measured at 10 nm and that of film B at 20 nm. This difference in their surface morphology and thickness was consistent with the fact that using low HF concentration electrolyte, the surface grows rougher and part of the layer is chemically dissolved in the electrolyte. High resolution TEM (HREM) images showed, in both films, Si nanocrystals embedded in an amorphous matrix (Fig. 1b). However, the nanocrystals in film B were on average smaller than in film A. Using X-ray and Ultra-violet photoelectron spectroscopies (XPS, UPS) we were able to monitor the oxidation levels at the outer surface and the internal surface of the films, revealed after sputtering (Fig. 2a). Using this information, we found that both types of films were porous and, most interestingly, film B at its outermost surface was composed of very tiny Si nanocrystals smaller than those in the internal surface. However, in film A Si nanocrystals were more uniform in depth regarding their size and generally larger than those in film B. Film B was light emitting, whereas film A was not, as it contained larger Si nanocrystals than film B. Detailed temperature dependent photoluminescence (PL) and time-resolved PL measurements showed that the light emission was due to exciton recombination in the Si nanocrystals with sizes less than 3 nm (Fig. 2b).

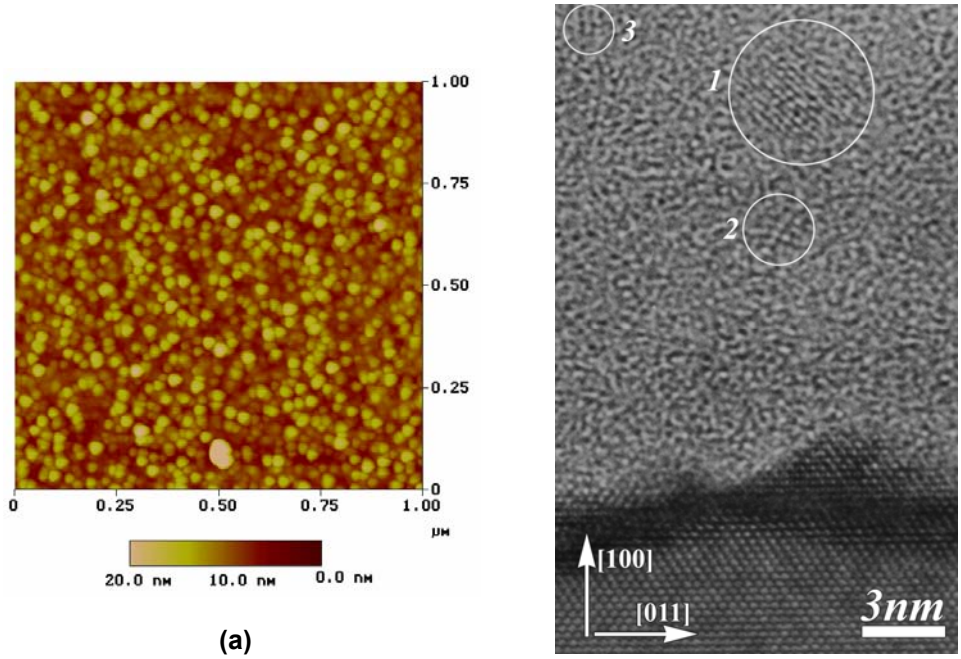


Fig. 1. (a) *AFM image showing the surface morphology of film A.* ***(b)*** *HREM image obtained from film A, showing Si nanocrystals (encircled) embedded in an amorphous matrix.*

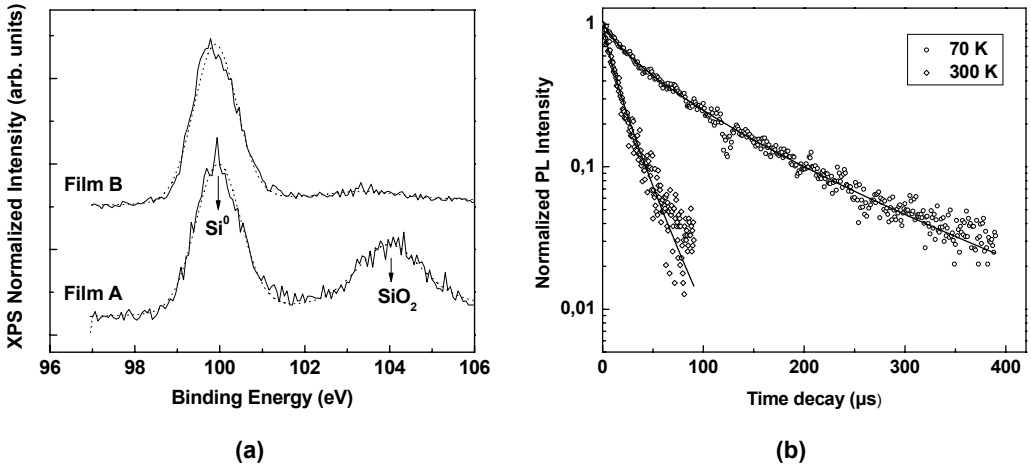


Fig. 2. (a) *Si-2p core level XPS spectra obtained from films A and B. The two spectra show the oxidation condition of the outermost surface of the two films. In film A the oxide layer is much thicker than that in film B.* ***(b)*** *PL time decay curves obtained at 70 K and 300 K. Both follow the stretched exponential law which characterizes disordered systems.*

C. Fabrication of porous anodic alumina on pre-selected areas on a Si substrate.

V. Gianneta and A. G. Nassiopoulou

Porous anodic alumina is a very interesting material because of the spontaneous formation of self organized arrays of pores under appropriate electrochemical conditions. Within this activity the electrochemical fabrication of porous anodic alumina (PAA) thin films on selected areas on Si substrate was developed. This is achieved by anodizing pre-patterneed aluminum thin films on Si. The aluminum films are anodized at various electrochemical conditions. It is shown that the confinement of the porous alumina membrane influences the ordering and the size of the thin porous alumina structure. The PAA films on pre-selected areas are appropriate for use as templates for growing metal or semiconductor nanowires or nanodots therein, for several applications in nanoelectronics, photonics and sensors.

Fig.1 shows a typical SEM image of the surface of porous anodic alumina thin films grown on the whole Si surface (a) and on confined areas on Si (b) in planar view (a_1, a_2) and in cross section (b_1, b_2) .

The size of the pores varied from 10 to 140 nm in diameter and 30 to 900 nm in height, depending on the electrochemical conditions used.

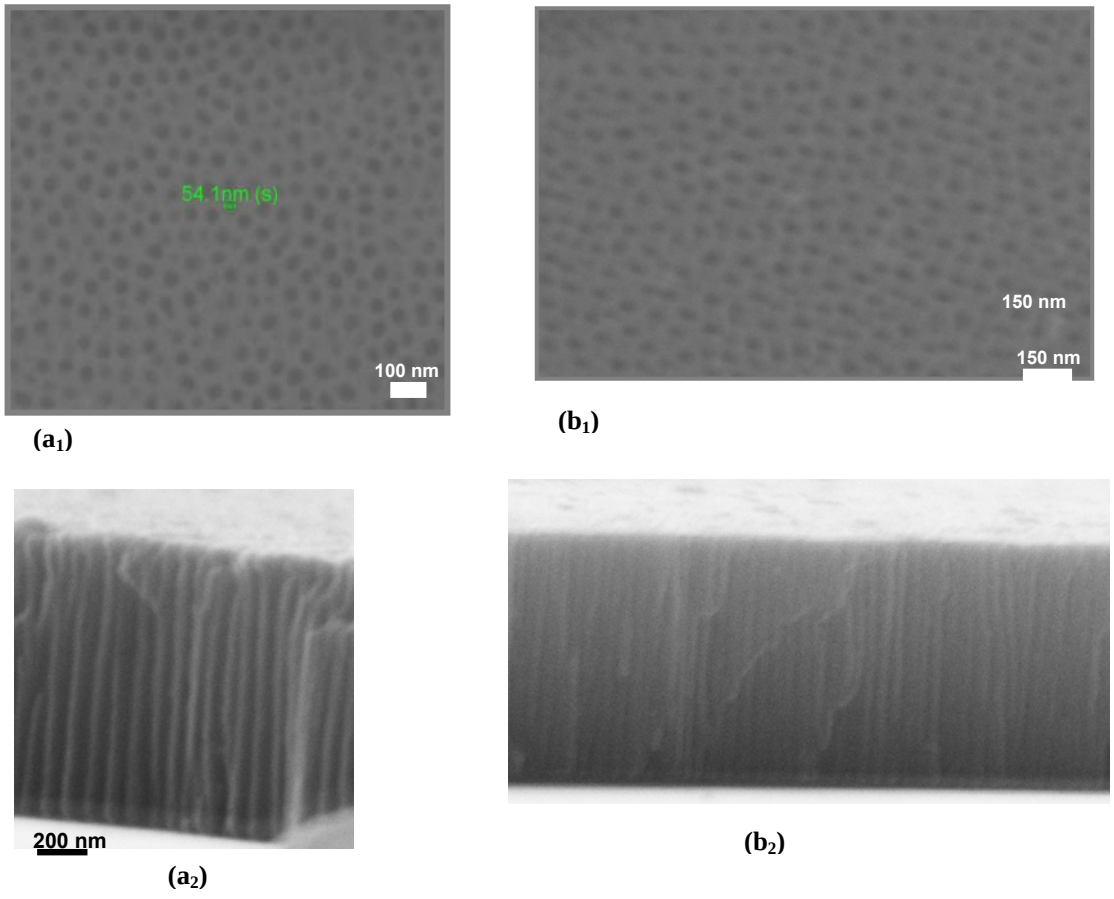


Fig. 1. *SEM images of porous anodic alumina fabricated by anodization of Al thin films on the whole Si surface (a) and on confined areas on Si (b). The pore diameter in the first case (Fig 1a) is 55 nm and in (b) (Fig 1b) is 33 nm for the same electrolytic conditions.*

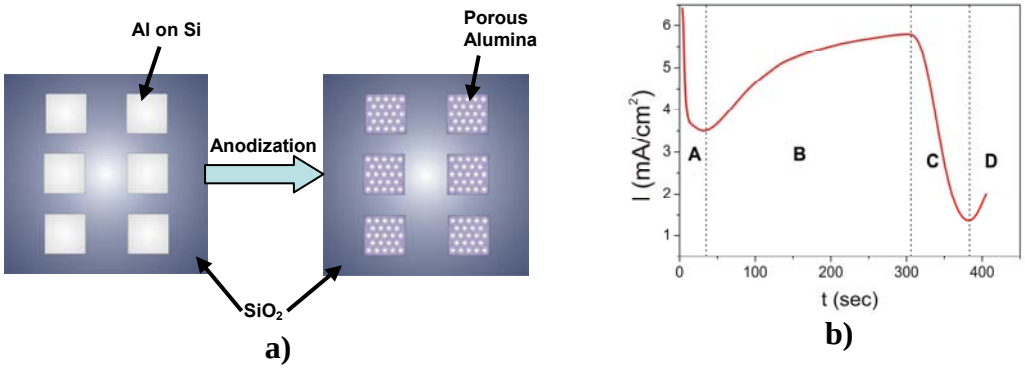


Fig. 2. (a) *Schematic representation of the fabrication process of porous anodic alumina thin films on pre-selected areas on Si (b) typical curve of current density versus time during anodization of Al films.*

Fig. 3 shows Ti dots fabricated on Si by sputtering of Ti thin film into a porous alumina thin film, used as template is presented. The image shows Ti dots after dissolution of the alumina template.

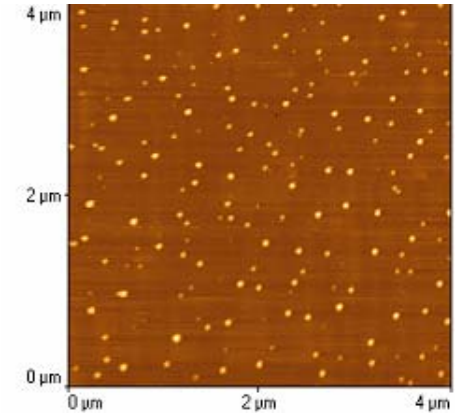


Fig. 3. (a) *AFM image of Ti dots and nanopillars on a Si substrate*

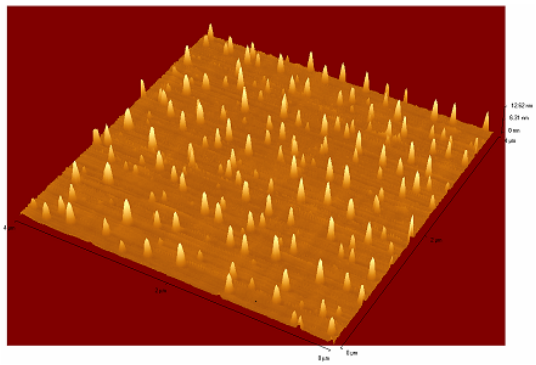


Fig. 3. (b) *AFM 3D image of Ti dots and nanopillars on a Si substrate*

Fig. 4 presents a similar sample of figs 3 sample, in which electrodeposition of Au ions on Ti dots took place.

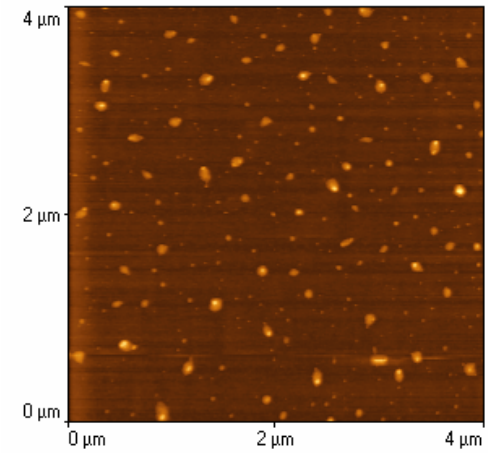


Fig. 4. (a) *AFM 2-D image of Au/Ti nanodots electrodeposited on Si using anodic porous alumina template technology*

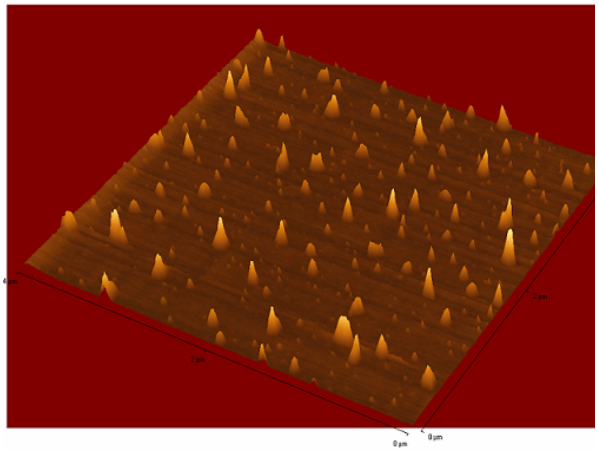


Fig. 4. (b) *AFM 3D image of Au/Ti nanodots electrodeposited on Si using anodic porous alumina template technology*

D. Patterning of Si substrates using porous-anodic-alumina-on-Si masking technology

F. Zacharatos, V. Gianneta and A. G. Nassiopoulou

Nano- and macroporous Si is a material grown on Si by electrochemistry. Under appropriate conditions the material shows vertical cylindrical pores. In order to introduce ordering in pore formation, pre-patterning of the Si surface is needed. We developed a Si pre-patterning technique using anodically grown porous anodic alumina films on Si as masking layers. p^+-type (100) Si wafers were used. The pores were arranged in a hexagonal close-packed structure, following the ordering of alumina pores. Pore initiation pits on Si were formed through the alumina template by HF anodic etching (semi-spherical pits) or by TMAH chemical etching (inverted pyramids), see Figs.1a-b.

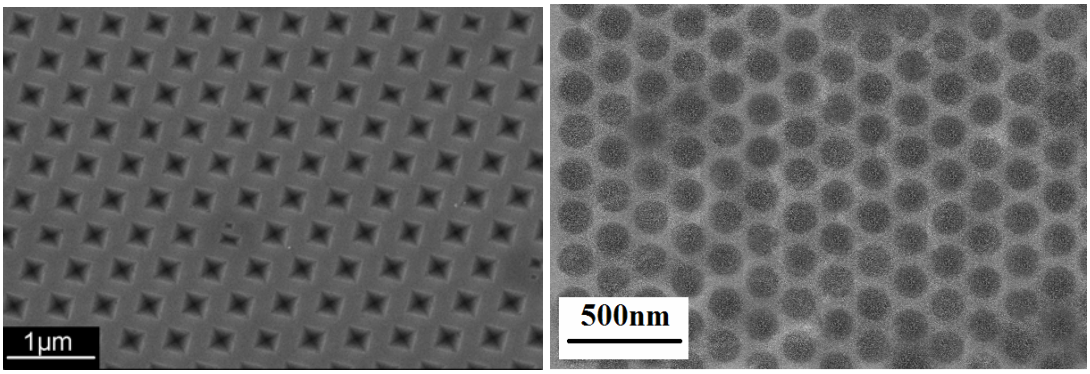


Fig.1. *SEM images of hexagonally ordered inverted pyramids* ***(a)*** *fabricated through PAA membrane by wet etching in a TMAH solution 25%w.t. at 80°C semispherical pits* ***(b)*** *following the arrangement of the PAA pores formed with electrolytic etching in a HF:H_2O:IP solution 3:6:10.*

Further electrochemical etching of the pre-patterned samples leads to deep macroporous Si membrane formation with vertical cylindrical pores hexagonally arranged on the Si substrate (Figs. 2a-b). Pore density is controlled by the electrochemical conditions used for the fabrication of the alumina template. Pore size was much smaller than in a structure with randomly distributed pores, fabricated under the same electrochemical conditions. We also observed that in the case of ordered pores the thickness of macropores walls was by a factor of 2 smaller than in the case of non-ordered pores and the structure was in general more closely packed, following pore initiation pits that determine the position of each pore and consequently the pore wall thickness.

The developed process offers high flexibility in the design of photonic crystals based on macro and nanoporous silicon.

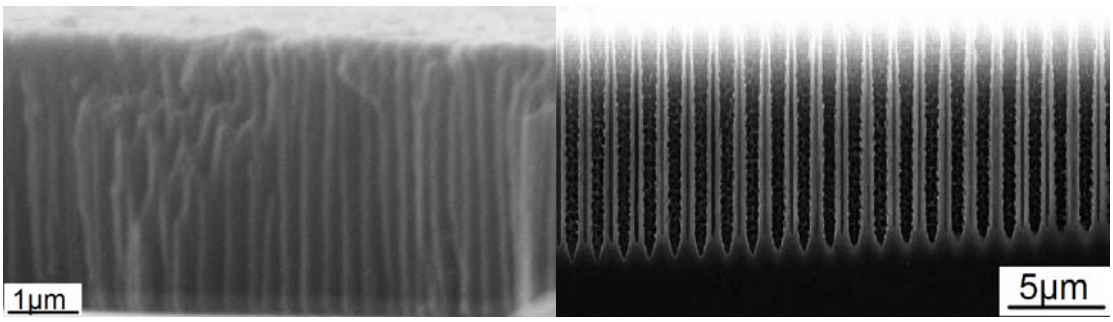


Fig. 2 *Cross-sectional SEM images of macroporous Si fabricated by electrochemical etching of pre-patterned Si surfaces as follows:* ***(a)*** *Etching of a p^+-type substrate in HF:ethanol 4:6 solution in volume.* ***(b)*** *Etching of a p-type substrates by electrochemical dissolution in an HF:DMF solution 12:88 in volume.*

E. Dielectric characterization of macroporous silicon thick layers for use as capacitors in high voltage applications

M. Theodoropoulou, D. N. Pagonis, A. G. Nassiopoulou
In collaboration with C. A. Krontiras and S. Georga from the University of Patras

Macroporous silicon composed of cylindrical macropores perpendicularly oriented on to the surface was fabricated on selected areas on a P+ silicon substrate (resistivity: 5mOhm.cm) by anodization in HF x Ethanol solution (40%-60% in volume) at a current density of 20 mA/cm^2. The thickness of the macroporous layer was 10μm. The samples were oxidized at high temperature in N_2 ambient in order to form SiO_2 of 20, 40 and 72 nm on pore walls and sample surface. MOS capacitors with Al metallization were then fabricated (Fig.1) and the samples were characterized by dielectric spectroscopy (DS) in the frequency range 1Hz - 1MHz and in the temperature range 173 - 353K. The results reveal that at low temperatures the dielectric constant ε΄ is independent of frequency (t_{ox}=20nm ε΄~ 3.4, t_{ox}=40nm ε΄~2.8, t_{ox}=72nm ε΄~ 2.6). Above a certain temperature, the dielectric constant increases versus temperature in the low frequency region (Fig.2). This behavior is attributed to the contribution of space charge carriers to the total dielectric response. A theoretical model, which calculates the static dielectric constant of the samples is proposed (Fig.3). The calculated theoretical values are in good agreement with the experimental ones. Dielectric loss data show that the oxidized samples exhibit values of tanδ <10^{-2} in the frequency range used, which are smaller than those of the non-oxidized samples (Fig.4). The obtained results open important perspectives in using oxidized macroporous silicon thick layers in capacitors for high voltage applications.

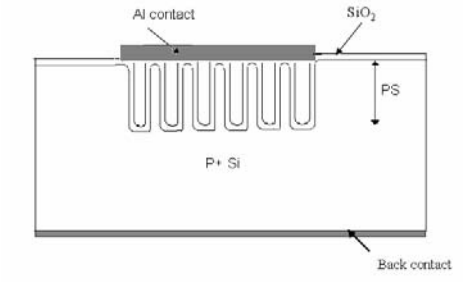


Fig.1. *Macroporous Si film on a Si substrate*

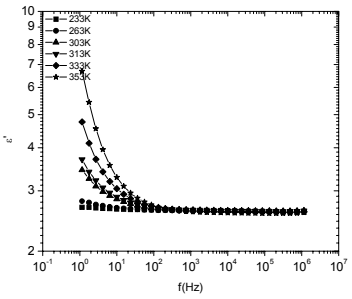


Fig.2. *Dielectric constant ε as a function of frequency at different temperatures*

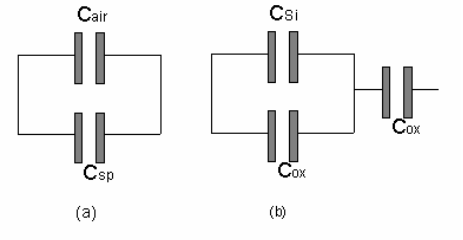


Fig.3. *Equivalent electrical circuit*

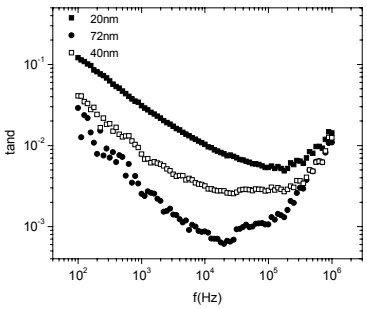


Fig.4. *Loss tangent as a function of frequency for 3 different film thicknesses*

$$\varepsilon_{MPS} = \varepsilon_{air} P + \varepsilon_{SP} (1-P)$$

$$\varepsilon_{sp} = \varepsilon_{Si} - \left(\frac{2t_{ox}}{t_{Si} + 1.1t_{ox}} \right) (\varepsilon_{Si} - \varepsilon_{ox})$$

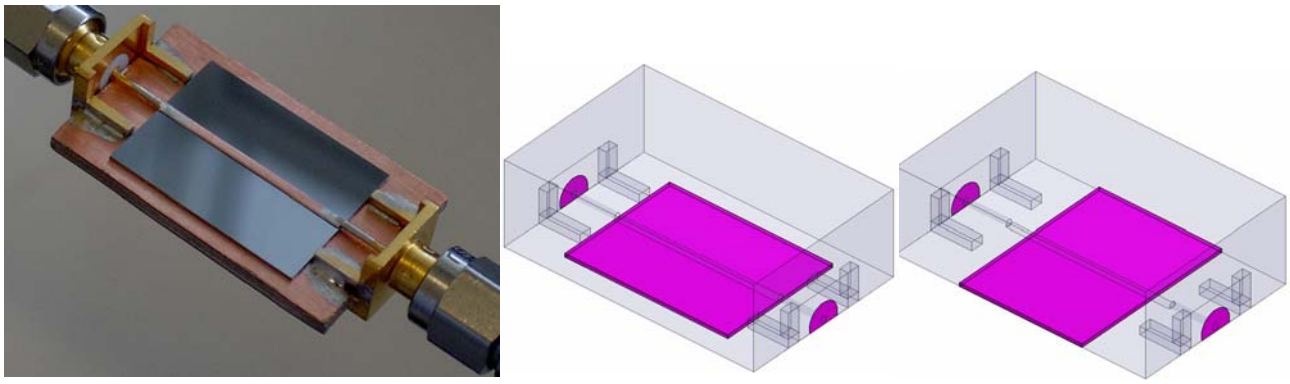
F. RF passives integrated on a porous Si microplate on the Si substrate. Porous material characterization at RF

H. Contopanagos, D. Pagonis and A. G. Nassiopoulou

A technology is under development at IMEL for the integration of RF passives on Si. It consists in Fabrication porous Si microplates locally on the Si substrate and integrate the RF passives on them. Porous Si shows very different properties than bulk Si and it appears to show low losses at RF. RF passives and high Q resonators may thus integrated on Si using porous Si as a local substrate. Different forms of porous Si are under investigation and different measuring systems were used. As an example, we will describe below measurements on macroporous Si using a macroscopic microstrip line method and on mesoporous Si using an on-chip coplanar waveguide.

F_1. *Complex permittivity extraction of macroporous Si by a macroscopic microstrip line method*

In this method, we have fabricated a macroscopic platform consisting of a grounded Roger's Duroid laminate on which coaxial connectors have been directly soldered creating a continuous, gapless ground plane. Then, a free-standing copper microstrip line is permanently soldered on the connectors. A wafer sample is inserted directly underneath the line. A picture of the fabricated macroscopic platform containing the grown sample, and HFSS simulator schematics are shown in Fig. 1.



(a) (b) (c)

Fig. 1. *(a) Macroscopic platform with wafer sample inserted.* ***(b)*** *Simulation layout in the b) long and* ***(c)*** *short orientation*

The method consists of measuring the 2-port S-parameters of the system in a given frequency range using a Vector Network Analyzer. Then, to theoretically simulate the same structure using a full-wave finite elements electromagnetics solver. In the simulations, we have to build exactly the geometry of the measured system, because the sample is not laterally infinite, and the connectors cannot be deembedded, hence analytical formulas pertaining to microstrip lines are inaccurate. We performed a series of simulations varying the unknown complex permittivity of the porous Si layer until the theoretical S-parameters best fit the measured ones. The dimensions of the platform are as follows:

Cu Ground: 30.6mm×20mm
Microstrip Line Ground Clearance: 0.380+(≈) 0.015mm
Connector Pin Radius: 0.375mm
Wafer: 20mm×15mm×0.380mm
Cu Microstrip Line: 20.6mm×1mm×0.05mm
Connector Length: 5mm
Connector Pin Ground Clearence: 0.25mm
Porous Si Layer Thickness: 50μm

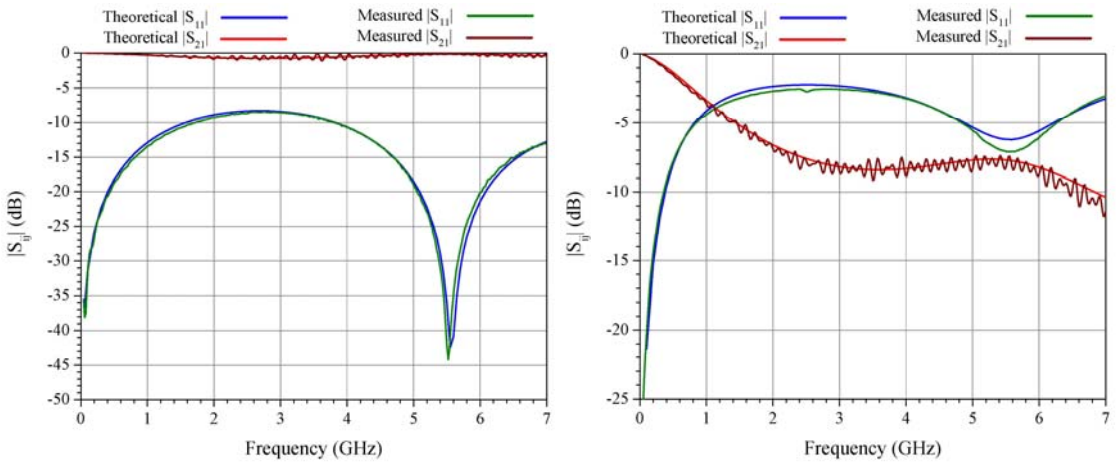


Fig. 2. ***(a)*** *Method validation for air platform.* ***(b)*** *Short orientation: 15mm × 20mm*

In Fig. 2a we compare theoretical vs measured results for the platform without the sample to validate the accuracy of the simulation and fabrication, to excellent agreement. In Fig. 2b we present an excellent fit between measured S-parameters versus theoretical ones, for a p^+ Si substrate of ρ = 8 Ω.cm. The extracted complex permittivity of macroporous Si is $\varepsilon_{pSi} = 4.9 \times (1 + i0.15)$.

F_2. *RF-shielding of mesoporous Si measured through an on-chip coplanar waveguide*

H. Contopanagos, F. Zacharatos and A. G. Nassiopoulou

In this work we have grown mesoporous Si microplates of various thicknesses, and have measured the corresponding losses within a broad range of frequencies. We have compared these losses to the corresponding losses when the same measuring platform is fabricated on a bare p-type Si die of ρ = 8 Ω.cm, of the kind used in standard CMOS. The measuring platform we have used is shown in Fig. 1 and is now at scales consistent with on-chip passive device fabrication. It consists of an on-chip Coplanar Waveguide (CPW) fabricated on a fixed-thickness Si die using Al metallization. The CPW has been optimized to present a well-matched transmission line to the 50Ω ports of the measurement set-up, taking into account the anticipated values of the permittivity of the mesoporous Si layer (inspired by the macroscopic measurements presented above). The dimensions for the results presented here are: L=5mm, G=780μm, S=80μm, g=35μm. The total die thickness is 380μm with any combination of porous Si layer thickness, while the Al metallization has a thickness of 0.5μm. The measurement set-up consisted of a Cascade RF prober with 100μm-pitch Ground-Signal-Ground (GSG) RF probes, and an Anritsu DC-40GHz Vector Network Analyzer.

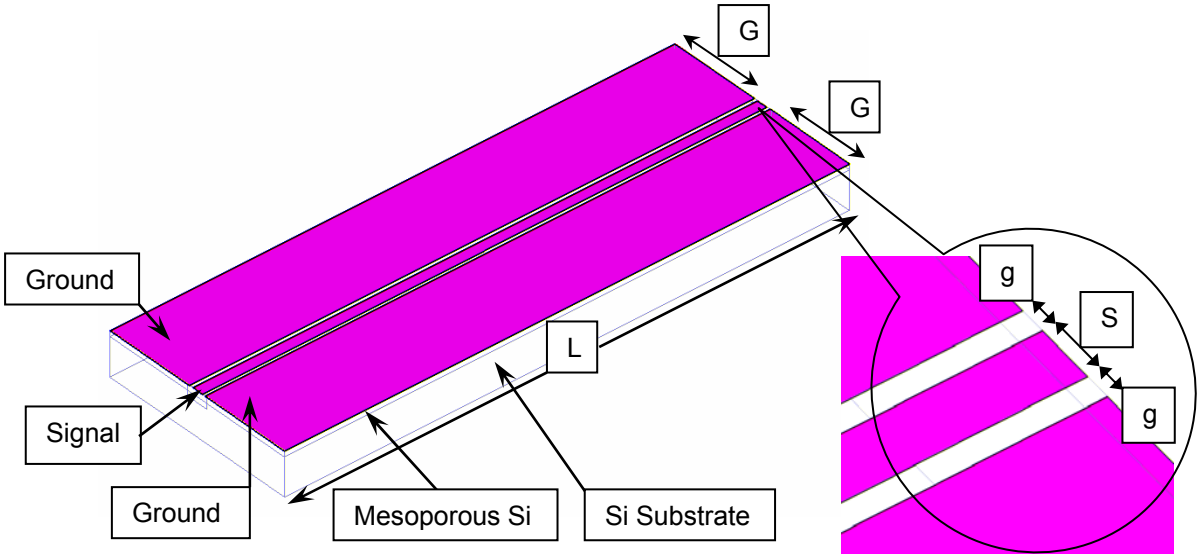


Fig. 1 *On-chip CPW platform metallized on a wafer sample*

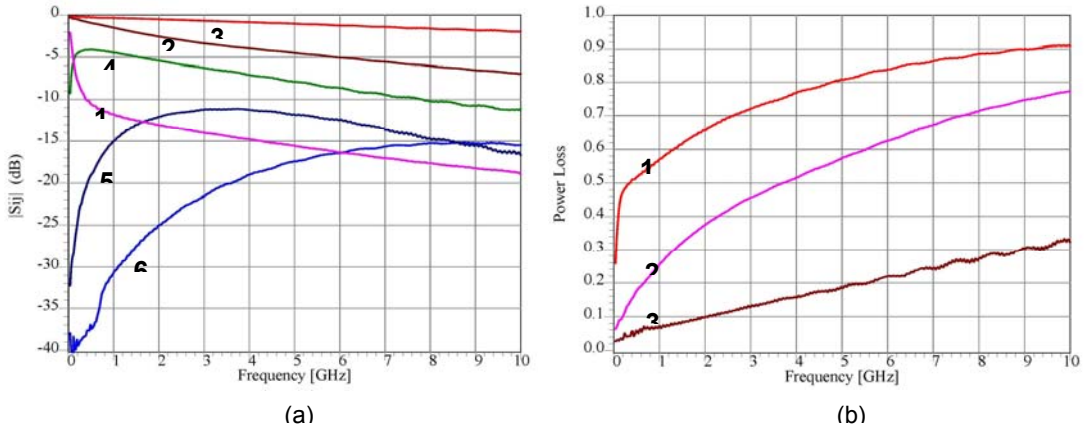


Fig. 2. ***(a)*** *Measured S-parameters (in dB's) for 3 different dies. Transmittivities ($|S_{21}|$) for: 1 no porous, 2 a 25μm-thick layer of mesoporous Si, 3 a 50 μm-thick mesoporous Si layer; Reflectivities ($|S_{11}|$) for: 4 no porous, 5 25μm -thick layer of mesoporous Si, 6 a 50 μm-thick mesoporous Si layer.* ***(b)*** *Measured Power Loss (PL) defined as PL=1-$|S_{11}|^2$-$|S_{21}|^2$, for: 1 no porous, 2 a 25μm-thick layer of mesoporous Si, 3 a 50 μm-thick mesoporous Si layer.*

In fig. 2a we present the measured scattering parameters of 3 identical CPW's fabricated on 3 different dies, all of the same total thickness. We see that without the porous the reflection is not large, even at low frequencies, but the line becomes better matched at higher frequencies. Despite that, the transmission is suppressed even at the DC limit and becomes quite small for increasing frequencies. On the contrary, when the thin porous microplate is introduced, the transmission jumps to substantial values while the reflection becomes very well matched throughout the frequency range (less than -10 dBs), and especially at low frequencies. Finally, with a 50-μm-thick microplate the reflection becomes negligible (below -15 dB's) providing excellent matching, while transmission is quite high. We notice in Fig. 2b that the bare Si die consumes a lot of power, starting at 50% at low frequencies and reaching 70-85% at the important Bluetooth-WLAN range of 2.5-5.5 GHz. The 25μm-thick porous microplate suppresses that loss, but doubling that thickness to 50μm substantially reduces the RF losses to 1/6-1/4 of the corresponding values in a bare, p-type Si die used in standard CMOS. Therefore, this material is excellent for CMOS-compatible integration of passive RF devices.

G. Theoretical investigation of the optical properties of metalodielectric micro and nanostructures

N. Papanikolaou (in collaboration with N. Stefanou from the University of Athens)

Modern nanofabrication methods and lithographic techniques have revealed new possibilities of manipulating light. New, very promising and exciting applications in non linear optics, optical filters, near field imaging and biological sensing, were successfully demonstrated over the last years. In particular the excitation of surface plasmon-polaritons (SP) offers new possibilities since at the resonance frequency the electromagnetic field is focused in subwavelenght volumes with increased intensity.
Plasmon excitations are also responsible for the effect of enhanced transmittance where light passes through optically thick metallic films perforated with a periodic array of holes smaller than the light wavelength. The transmitted intensity is higher than the one predicted for normal diffraction. Similar effects were observed also in films without holes. We have investigated theoretically the effect of enhanced transmittance through Ag films without holes interacting with a periodic array of metallic spheres in close contact. We predicted enhanced transmittance through the film and investigated different parameters influencing the effect.

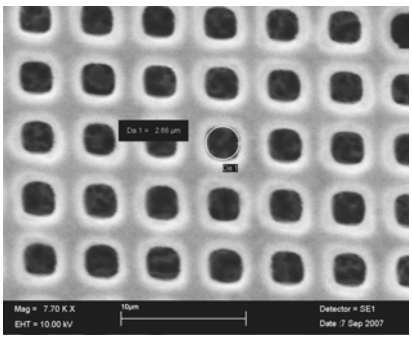


Fig. 1. *SEM micro-graph of the structures prepared by optical lithography: A square array of holes on a Si substrate covered with a 100 nm thick Al film. The hole diameter is 2.7 μm and the lattice constant 5μm.*

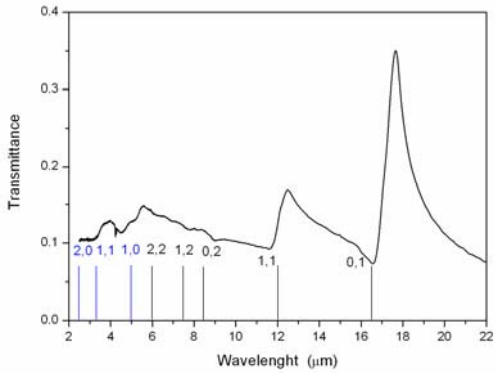


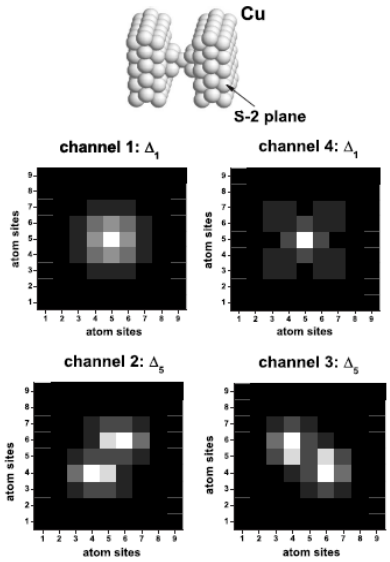
Fig. 2. *Transmission spectra of 100nm Al films patterned with a periodic array of square holes (lattice constant a=5 μm, hole diameter d=3.2μm). The film lies on a uniform Si substrate, the horizontal lines denote SP frequencies for Si/Al (black, full lines), and Si/air(blue, dashed lines)*

Similar enhanced transmittance can be observed also in the infrared for micrometer size structures. We constructed photonic structures using conventional Si technologies. A square lattice of holes on a Si waver covered with a thin layer of metal (Al or Au) is shown in Fig. 1. The perforated metallic array shows extraordinary transmittance up to 35% (Figure 2) for wavelengths bigger than the size of the holes. Finally the pattern was transferred in the Si substrate using plasma etching. The final structures show absorption in a narrow band for wavelengths close to the lattice constants and are examined for possible use as efficient infrared emitters.

Electronic transport in few atom atomic contacts using *ab initio* electronic structure calculations

Understanding electronic transport in the atomic scale is an important milestone towards molecural electronic devices. The invention of the scanning tunneling microscope in 1981 and a consequent development in the beginning of the 1990s of the remarkably simple experimental technique known as mechanically controllable break junction led to the possibility of fabricating metallic point contacts approaching the atomic scale. In the experiments, the conductance measured as a function of the elongation of the nanocontacts decreases in a stepwise fashion, with steps of order of the conductance quantum $G0=2e^2/h$. Such behavior of the conductance is attributed to atomic rearrangements that entail a discrete

variation of the contact diameter. We develop formalism for the evaluation of conduction eigenchannels of atomic-sized contacts from first principles.



Electron probability densities of the four dominating eigenchannels for the pyramidal Cu contact shown on the top. Wave functions resolved to atoms are visualized two atomic planes below the surface plane S-1. Colors from white to black correspond to consequently decreasing positive values. Transmission probabilities of channels are T1=0.90, T2=T3=0.71, and T4=0.08 , which are summed up to conductance G =2.57G0.

The multiple scattering Korringa-Kohn-Rostoker Green's function method is combined with the Kubo linear response theory. Solutions of the eigenvalue problem for the transmission matrix are proven to be identical to eigenchannels introduced by Landauer and Büttiker. Applications of the method are presented by studying ballistic electron transport through different single atom metallic contacts. In the figures we show the decomposition of the conductance in different channels and the spatial distribution of the electron probability in each channel for a Cu contact.

PROJECT OUTPUT IN 2007

LIST OF PUBLICATIONS IN REFEREED JOURNALS

1. "Influence of grain size on ultrafast carrier dynamics in thin nanocrystalline silicon films", E. Lioudakisa, A. Othonos, A. G. Nassiopoulou, Ch. B. Lioutas and N. Frangis, Appl. Phys. Lett. 90, 191114 2007
2. "Ultrafast transient photoinduced absorption in silicon nanocrystals: Coupling of oxygen-related states to quantized sublevels", E. Lioudakisa, A. Othonos, A. G. Nassiopoulou, Appl. Phys. Lett. 90, 171103 2007
3. "Quntum confinement and interface structure of Si nanocrystals of sizes 3-5 nm embedded in α-SiO2" E. Lioudakis, A. Othonos, G. C. Hadjisavvas, P. C. Kelires and A. G. Nassiopoulou" Physica E 38 128-134 (2007)
4. "Charging/discharging kinetics in LPCVD silicon nanocrystal MOS memory structures" V. Turchanikov, A. Nazarov, V. Lysenko, E. Tsoi, A. Salonidou and A. G. Nassiopoulou Physia E 38 89-93 (2007)
5. "Nanostructuring Si surface and Si/SiO2 interface using porous-alumina-on-Si template technology. Electrical characterization of Si/SiO2 interface" M. Kokonou, A. G. Nassiopoulou, Physica E 38, 1-5 (2007)
6. "Fundamental transport processes in assembles of silicon quantum dots" I. Balberg, E. Savir, J. Jedrzejewski, A. G. Nassiopoulou, S. Gardelis, Phys. Rev. B 75 235329 (2007)
7. "Ultrafast transient photoinduced absorption in silicon nanocrystals:Coupling of oxygen-related states to quantized sub-levels" E. Lioudakis, A. Othonos and A. G. Nassiopoulou Appl. Phys. Lett. 90 171103 (2007)
8. "Self-assembly of single thin Au nanoparticle chains on Si along V-groove-etched lines between micrometer-distant electrodes by dielectrophoresis" A. Zoy, A. A. Nassiopoulos and A. G. Nassiopoulou Nanotechnology 18 345608 (2007)
9. "Two-silicon-nanocrystal layer memory structure with improved retention characteristics", A. G. Nassiopoulou and A. Salonidou, J. Nanosci. Nanotechnol., vol. 7, 368-373 (2007)

10. “Ge quantum dot memory structure with laterally ordered highly dense arrays of Ge dots”, A. G. Nassiopoulou, A. Olzierski, E. Tsoi, I. Berbezier and A. Karmous, J. Nanosci. Nanotechnol., vol. 7, 316-321 (2007)
11. "The role of surface vibrations and quantum confinement effect to the optical properties of very thin nanocrystalline silicon films", Lioudakis, E., Antoniou, A., Othonos, A., Christofides, C., Nassiopoulou, A.G., Lioutas, Ch.B., Frangis, N., J. of Appl. Physics 102 (8), art. no. 083534 (2007)
12. "Ultra-thin films with embedded Si nanocrystals fabricated by electrochemical dissolution of bulk crystalline Si in the transition regime between porosification and electropolishing", Gardelis, S., Tsiaoussis, I., Frangis, N., Nassiopoulou, A.G., Nanotechnology 18 (11), art. no. 115705 (2007)
13. "Few nanometer thick anodic porous alumina films on silicon with high density of vertical pores", Kokonou M., Giannakopoulos K.P., Nassiopoulou A.G., Thin Solid Films 515(7-8), 3602-3606(2007)
14. "A smart flow measurement system for flow evaluation with multiple signals in different operation modes", G Kaltsas, P Katsikogiannis, P Asimakopoulos, A G Nassiopoulou, Meas. Sci. Technol. 18 (2007) 3617–3624
15. "A silicon thermal accelerometer without solid proof mass using porous silicon thermal isolation" D. Goustouridis, G. Kaltsas and A. G. Nassiopoulou IEEE Sensors Journal, vol. 7 No 7 983 (2007)
16. "Formation of confined macroporous silicon membranes on pre-defined areas on the Si substrate", Pagonis, D.N., Nassiopoulou, A.G., Physica Status Solidi (A) Applications and Materials 204 (5), pp. 1335-1339 (2007)
17. "Novel microfluidic flow sensor based on a microchannel capped by porous silicon", Pagonis, D.N., Petropoulos, A., Kaltsas, G., Nassiopoulou, A.G., Tserepi, A., Physica Status Solidi (A) Applications and Materials 204 (5), pp. 1474-1479 (2007)
18. "Integrated inductors on porous silicon", Contopanagos, H., Nassiopoulou, A.G., Physica Status Solidi (A) Applications and Materials 204 (5), pp. 1454-1458 (2007)

PAPERS IN CONFERENCE PROCEEDINGS

1. "Nanostructuring SiO2/Si(100) surface for lateral ordering of self-assembled semiconductor quantum dots" (invited) A. G. Nassiopoulou and M. Kokonou, Physics, Chemistry and Applications of Nanostructures, World Scientific Publishing, Edited by V E Borisenko, S V Gaponenko and V S Gurin p. 407 (2007)
2. "Structural and light-emitting properties of ultra thin anodic silicon films formed at the early stages of bulk silicon anodization" (invited) S. Gardelis, A. G. Nassiopoulou, I. Tsiaoussis and N. Frangis, Physics, Chemistry and Applications of Nanostructures, World Scientific Publishing, Edited by V E Borisenko, S V Gaponenko and V S Gurin p. 407 (2007)
3. "Spectroscopic characterization of thin anodic silicon layers grown by short monopulses of current", Gardelis, S., Jaziri, S., Nassiopoulou, A.G., AIP Conference Proceedings 935, pp. 87-91 (2007)
4. "A novel microfabrication technology on organic substrates - Application to a thermal flow sensor", G. Kaltsas, A. Petropoulos, K. Tsougeni, D. N. Pagonis, T. Speliotis, E. Gogolides and A. G. Nassiopoulou, Journal of Physics: Conference Series 92 (2007) 012046

CONFERENCE PRESENTATIONS

1. "Nanopatterning the Si Surface Through Porous Anodic Alumina Masking Layers", F. Zacharatos, V. Gianneta, A. G. Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
2. "Determination of critical points of nanocrystalline silicon films: the role of grain boundaries in the optical properties", E. Lioudakis, A. Othonos and A. G. Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
3. "Monitor the properties of silicon nanocrystals embedded in SiO2 matrix using ultrashort laser pulses", E.Lioudakis, A. Othonos, A. Emporas and A. G. Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
4. "Anodic Porous Alumina Thin Films on Si: Interface Characterization", V. Gianneta, S. N. Georga, C. A. Krontiras, A. G Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
5. "Auger Recombination in Silicon Nanocrystals", M. Mahdouani, R. Bourguiga, S. Jaziri, S. Gardelis, A.G. Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology & MEMs, held at NCSR “Demokritos”, 18-21 November 2007
6. "Assembly and electrical investigation of tiopronin- and citrate-stabilized Au nanoparticle chains between electrodes on patterned oxidized Si substrates under the influence of an electric field", A Zoy and A G Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
7. "TEM characterization of ultra-thin nanocrystalline Si films grown on quartz and presenting quantum properties", Ch.B. Lioutas, N. Vouroutzis, I. Tsiaoussis, N. Frangis and A.G. Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007

8. "Structural study of ultra thin anodic silicon layers for nanoelectronic and photonic applications", S. Gardelis, F. Petraki, S. Kennou, A. G. Nassiopoulou, 3rd International Conference Micro & Nano 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
9. "Broadband Electrical characterization of Porous Silicon at Microwave Frequencies", H. Contopanagos, D. Pagonis, A. G. Nassiopoulou, 3rd International Conf. "Micro & Nano" 2007 on
10. "A thermal vacuum detector fabricated by a combination of MEMS and PCB technologies", A. Petropoulos, G. Kaltsas, A. G. Nassiopoulou, 3rd International Conf. "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology & MEMs, held at NCSR “Demokritos”, 18-21 November 2007
11. "Fabrication and evaluation of a gas flow sensor, implemented on organic substrates by a novel integration technology", A. Petropoulos, G. Kaltsas, A. G. Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
12. "Copper Wires in Macroporous Si Template for Microchannel Heat Sink Technology", F. Zacharatos and A. G. Nassiopoulou, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007
13. "Dielectric Characterization of Macroporous Silicon Thick Layers For Use As Capacitors In High Voltage Application", M. Theodoropoulou, D. N. Pagonis, A. G. Nassiopoulou, C. A. Krontiras, S. N. Georga, 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007

INVITED TALKS

1. "Ordering of Si and Ge nanocrystals in 2-D layers for nanodot memory devices", A. G. Nassiopoulou **(invited talk)**, International Conference on Physics, Chemistry and Applications of Nanostructures, Nanomeeting 2007, Belarus, 22-25 May 2007
2. "Structural and light-emitting properties of ultra thin anodic silicon films formed at the early stages of anodization of bulk silicon", S. Gardelis **(invited talk)**, International Conference on Physics, Chemistry and Applications of Nanostructures, Nanomeeting 2007, Belarus, 22-25 May 2007
3. "Self-assembly of Si nanostructures on nanopatterned substrates: Application in nanocrystal memories" **(invited talk)** A. G. Nassiopoulou, 4th International Workshop on Nanosciences & Nanotechnologies (N&N07), Thessaloniki, 16-18 July 2007
4. "Silicon Nanocrystals embedded in SiO2: Optical and transport properties" A. G. Nassiopoulou **(invited talk)**, 2nd European Optical Society Topical Meeting on Optical Microsystems, Italy, 30 September – 3 October 2007
5. "Characterization of Silicon Nanocrystal non-Volatile Memory Structures with Double Nanocrystal Layers", A. G. Nassiopoulou **(invited talk)**, ANNA-Analytical Network for Nanotech, held at Munich, 29 November 2007
6. "Microelectronics beyond Moore" A. G. Nassiopoulou, **(invited talk)**, Summer Scool NCSR Demokritos, 9-20 July 2007

PhD THESES

1. "Growth and electrical characterization of Au nanowires between electrodes", PhD thesis: Argyro Zoy, Thesis supervisor: Dr A. G. Nassiopoulou, Examination: National Technical University of Athens, 7-9-2007, Examination Committee:
   - Assoc. Prof. D. Tsoukalas, NTUA-Athens
   - Assoc. Prof. S. Georga, University of Patras,
   - Prof. E. Liarokapis, NTUA, Athens
   - Dr A. G. Nassiopoulou, Director of Research, IMEL/NCSR Demokritos
   - Prof. P. Pissis, NTUA, Athens
   - Assoc. Prof. I. S. Raptis, NTUA, Athens

ORGANIZATION OF CONFERENCES, SYMPOSIA, WORKSHOPS

1. 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007. Chairperson of the Conference was Dr Androula G. Nassiopoulou

2. 3rd International Conference "Micro & Nano" 2007 on Micro-Nanoelectronics, Nanotechnology and MEMs, held at NCSR “Demokritos”, 18-21 November 2007. Chairperson of the Conference was Dr Androula G. Nassiopoulou