Project II.2

MATERIALS AND DEVICES FOR MEMORY APPLICATIONS

This new title of project II.2 (instead of nanocrystal memories) is more representative of our last 2 year-activities

Project leader: P.Normand

Key researchers: P. Normand, V. Ioannou-Sougleridis, P. Dimitrakis
Collaborating Researchers: P. Argitis, N. Glezos
Post-doctorals: E. Kapetanakis, V. Em. Vamvakas
PhD candidate: P. Goupidenis

Objectives

- Development of high-throughput synthesis routes to create functional dielectrics and nanostructured materials for electronic memory applications.
- Study of the structural and electrical properties of the generated materials and demonstration of material functionality enabling the development of low-voltage high-density memory devices.
- Realization and testing of memory devices and manufacturability assessment of the developed fabrication routes in an industrial environment.

Funding

- NEON, Nanocrystals for Electronic Applications, EU GROWTH GRD1, No 25619
- Bilateral French-Greek Project, Si-Nanocrystal Synthesis by Plasma-Immersion Ion-Implantation for Non-Volatile Memory Applications, EPAN. M.4.3.6.1E.

Activities

Our research activities in generating and evaluating new materials and structures for memory applications started in 1996 with the development of the low-energy ion-beam-synthesis (LE-IBS) technique. Two-dimensional arrays of Si nanocrystals in thin gate dielectrics were demonstrated and successfully exploited in the fabrication of nanocrystal memories (NCMs). This activity was first supported by the EU project, FASEM (1997-2000). LE-IBS development with target the realization of non-volatile NCMs in an industrial environment has been conducted further within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last five years for examining novel NCMs alternatives including: (a) Memory devices by Si^+ irradiation through poly-Si/SiO_2 gate stack in collaboration with FZR and ZMD AG both sited in Dresden (DE), (b) Memory devices using Ge-NCs produced by MBE in collaboration with Aarhus Univ. (DK), (c) hybrid silicon-organic and SiGe-organic memories in collaboration with Durham Univ. (UK); this last activity was conducted within the framework of the EU IST-FET project, FRACTURE (2001-2003), (d) formation of LE-IBS Ge-NCs in high-k dielectrics in collaboration with CEMES/CNRS (FR), FZR Dresden and CambridgeNanoTech (USA).

In 2007, our main activities focused on the following tasks: (A) Wet oxidation of silicon nitride implanted with low-energy Si ions for ONO memory stacks in collaboration with CEMES/CNRS and MDM-INFM (IT), (B) MOS structures with low-energy Ge-implanted thin gate oxides in collaboration with LETI/CEA (FR), (C) Room-temperature silicon oxidation by high-density helicon plasma reactor, in collaboration with project I.2 and NTUA (GR), (D) Proton radiation tolerance of nanocrystal memories in collaboration with NTUA and, (E) Formation of Si nanocrystals in thin SiO_2 layers by PIII in collaboration with CEMES/CNRS and Ion-Beam-Services (IBS, French SME).

RESEARCH RESULTS

A. Wet oxidation of silicon nitride implanted with low-energy Si ions for ONO memory stacks

V. Ioannou-Sougleridis, P. Dimitrakis, V. Em. Vamvakas, P. Normand

Nitride-based memory technology has the potential to fulfill the stringent requirements of non-volatile memory cell downscaling. This technology exploits the presence of discrete charge storage nodes in the form of deep traps distributed in nitride materials. Due to its promising in terms of scalability, the conventional SONOS (poly-Silicon/Oxide/Nitride/Oxide/Silicon) memory cell has today regained a lot of attention. Typical fabrication of the ONO stack consists in the growth of a thin SiO_2 layer on a Si substrate and subsequent deposition of a Si_3N_4 layer. The top silicon oxide is obtained either by deposition techniques or high-temperature wet oxidation of the Si_3N_4 layer. The latter approach has two main advantages. First, the quality of a thermal top oxide is higher in comparison to that of a deposited oxide. Second, during the oxidation step a silicon oxynitride transition layer containing a high density of traps forms between the top oxide and the remaining silicon nitride.

However, fabrication of functional thermal blocking oxides requires high oxidation temperatures (typically within the 1000°C range). For deep-submicron integration purposes, it is important to explore new technological routes that could lead to the formation of a thermal top oxide at lower oxidation temperatures. In this direction, we proposed in collaboration with CEMES/CNRS and MDM-CN-INFM, an alternative method that combines low-energy (1 keV) silicon ion implantation into a thin nitride-oxide (NO) stack and subsequent low-temperature wet oxidation (~850°C). TEM imaging and ToF-SIMS analysis (see Figs.II.2.1) show that for an implanted dose of $1.5x10^{16}$ Si cm^{-2}, (1) a 8nm-thick SiO_2 layer develops on the NO surface while in the case of unimplanted NO stack, the SiO_2 thickness does not exceed 3nm, (2) transformation of the implanted silicon nitride to oxygen-rich silicon nitride materials and (3) pilling-up of nitrogen atoms at the Si/SiO_2 interface. The resulting ONO stack exhibits strong charge storage effects and excellent charge retention properties leading to a 1.5 V 10-year extrapolated memory window at 125°C (Fig. II.2.2). These results suggest that this new fabrication route may lead to gate dielectric stacks of substantial impact for mainstream nitride-based memory devices.

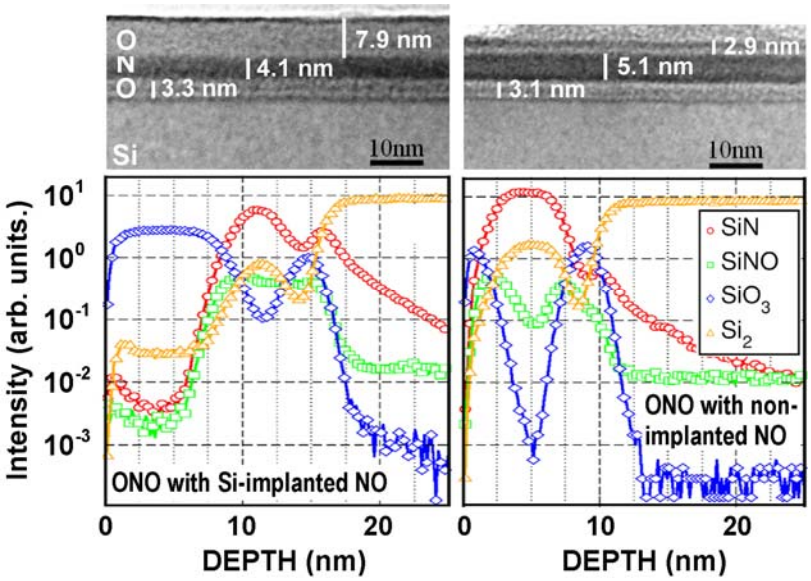

Fig. II.2.1: *TEM images and ToF-SIMS depth profiles of wet oxidized Si implanted (left) and non-implanted (right) nitride-oxide stacks.*

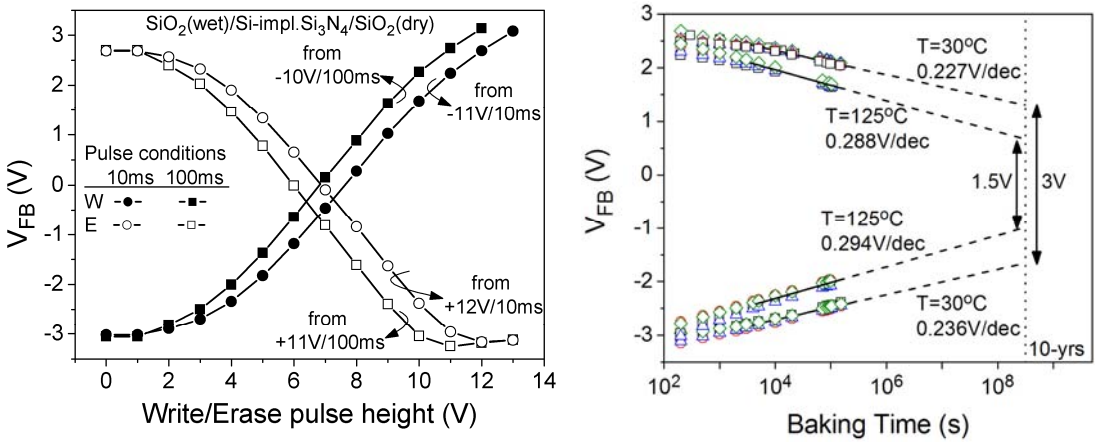

Fig. II.2.2: *Write/Erase (left) and charge retention (right) characteristics of ONO capacitors obtained by wet oxidation of Si implanted nitride-oxide stacks.*

B. MOS structures with low-energy Ge-implanted thin gate oxides

E. Kapetanakis and P. Normand

During the last few years, part of our research activities was concentrated on the formation of Si nanocrystals in thin oxide layers by low-energy (typically 1keV) ion-beam-synthesis (LE-IBS). Advances in fabrication allowed for overcoming several technological issues and successfully exploit LE-IBS to built low-voltage non-volatile Si-nanocrystal memories. In contrast to Si-implanted oxides, no clear indications of phase separation or other contrast were detected within low-energy (3keV) Ge-implanted and annealed SiO_2 films. In the latter case, phase separation of the implanted material has been observed only under long-time TEM electron irradiation conditions. The latter allowed for concluding that most of the Ge stays distributed within a band instead of forming separate pockets (e.g. in the form of Ge nanocrystals).

This year we focused our efforts on the electrical characteristics of MOS capacitors using 3 keV Ge-implanted and annealed thin gate oxides. Capacitance measurements at flat-band voltage before and after application of constant voltage stress in the accumulation regime indicate that the charge trapping behavior of the devices undergoes a major change after annealing at temperatures higher than 910^{o}C. The latter change was identified as a relocation of Ge atoms mainly towards the upper portion of the oxide with a significant fraction of them leaving the oxide; a finding in harmony with SIMS measurements (Fig. II.2.3) performed at LETI/CEA. The interface trap density (D_{it}) for the thin (9-12 nm) implanted oxides decreases with increasing annealing temperature, approaching at 950^{o}C, the D_{it} levels in the mid-$10^{10}eV^{-1}cm^{-2}$ range of the non-implanted samples.

At elevated annealing temperatures (> 1000^{o}C), the device C-V characteristics are substantially disturbed. In this case, the presence of electrically active Ge atoms at an extended depth in the substrate modifies the intrinsic electrical properties of the *n-type* Si substrate, lending a *p-type* conductivity character to the device high-frequency C-V curves (Fig. II.2.4). Substrate electrical modification was interpreted through a model that takes into account the formation of a SiO_2/Ge-rich-Si/n-Si system. The SiO_2/Ge-rich-Si interface presents very low D_{it} levels as revealed by conductance loss characteristics. The present study suggests that a combination of Ge implantation into SiO_2 thin films and thermal annealing may be exploited in damage-free SiGe epitaxial growth technology based on Ge implantation.

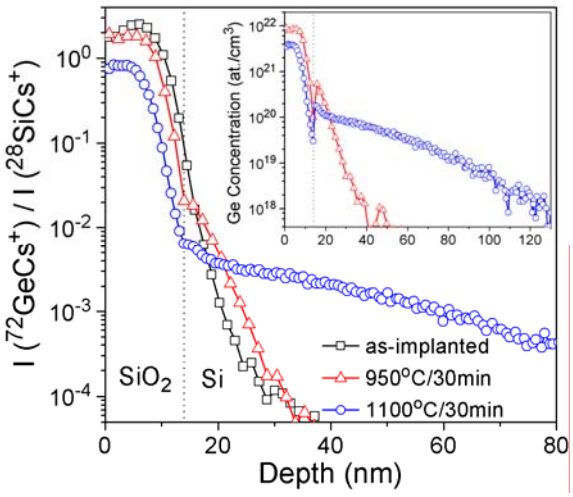

Fig. II.2.3: *^{72}GeCs$^+$ signals normalized to ^{28}SiCs$^+$ signals for 12nm-thick SiO_2 films implanted with 3 keV ^{72}Ge ions to a dose of 10^{16} cm^{-2} and annealed at 950 or 1100°C for 30 min. Inset: Extracted Ge concentration profiles for the annealed samples.*

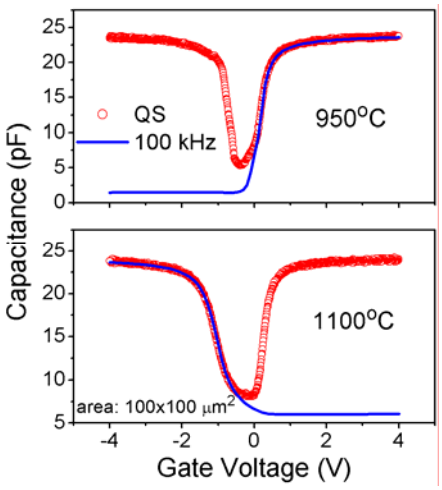

Fig. II.2.4: *Quasistatic and high-frequency C-V characteristics of MOS structures with 1×10^{16} Ge$^+$ cm^{-2} implanted gate SiO_2 of 12nm nominal thickness as a function of post-implantation annealing treatment.*

C. Room-temperature silicon oxidation by high-density helicon plasma reactor

M-E. Vlachopoulou, P. Dimitrakis, A. Tserepi, V. Em.Vamvakas, S. Koliopoulou, P. Normand, E. Gogolides, D. Tsoukalas[*]

[*]*National Technical University of Athens*

The physical and technical problems associated with the thermal growth of very thin silicon oxide layers in deep-submicron CMOS technology opened the opportunities either for exploring new dielectric materials or investigating low-thermal budget oxidation processes. In this direction, plasma oxidation (PO) of silicon appears attractive as it offers the rapid growth of an oxide film with good insulating properties at low processing temperatures. In collaboration with people from project I.2, we recently developed a room temperature PO process for producing silicon oxide films thinner than 8nm as gate oxides of MOSFET devices.

Silicon-PO experiments have been carried-out in a high-density helicon plasma reactor utilizing a gas mixture of Ar/O2, with oxygen partial pressure of about 1.5%. Silicon oxide films with a thickness in the 4-7nm range were successfully produced. Oxide thickness increases with plasma exposure time and substrate bias (Fig. II.2.5); thus indicating that oxide growth is an ion-enhanced process. The electrical properties of the PO produced oxides were evaluated using MOS capacitors. Typical high-frequency (1MHz) C-V characteristics of a 7nm-thick oxide layer after forming-gas post-metallization annealing (FG-PMA) are shown in Fig.II.2.6 and compared to those of a thermally grown dry oxide. It should be here emphasized that the FG-PMA improves substantially the quality of the as-grown oxides. PO was utilized to fabricate gate oxides of SOI-MOSFETs. Inset of Fig.II.2.6 shows typical output characteristics of the tested transistors at various front gate voltages (V_{GF}) with back-gate bias V_{GB}=0V. High current and low-leakage can be achieved at saturation regime, indicating good functionality of the plasma gate oxides.

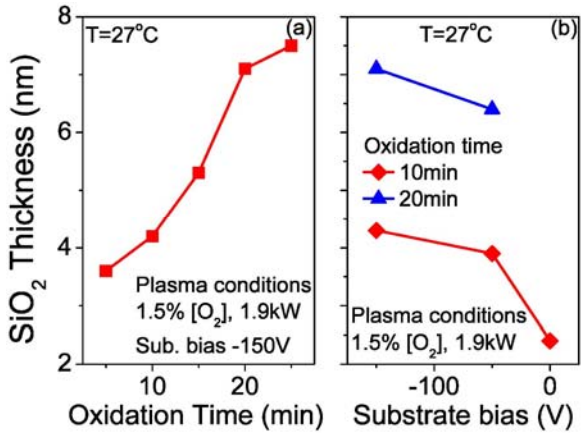

***Fig. II.2.5**: Plasma oxide thickness as a function of (a) PO time at fixed V_{BS}=-150V and (b) V_{BS} for 10min and 20min PO times.*

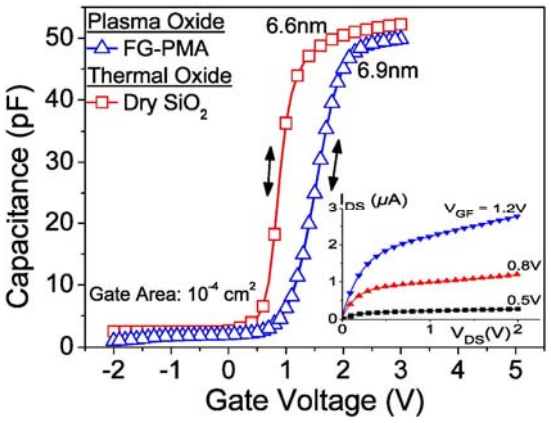

***Fig. II.2.6**: C-V plots (1MHz) for plasma oxide and thermal oxide MOS capacitors after FG-PMA. Inset: Typical output-characteristics of SOI-MOSFET with 2μm gate length and 10μm gate width using 7nm-thick plasma oxide.*

D. Proton radiation tolerance of nanocrystal memories

E. Verrelli, I. Anastassiadis*, D. Tsoukalas*, M. Kokkoris*, R. Vlastou*, P. Dimitrakis, P. Normand*

**National Technical University of Athens*

Radiation environments are encountered in military applications, nuclear power stations, nuclear waste disposal sites, high-altitude avionics, medical and space applications. Radiation type, energy, dose rate and total dose may be very different in each of these application areas and require in many cases radiation-tolerant electronic systems. The way radiation damages electronic systems depends strongly on the environment and can be classified as total ionizing dose effects (TID) and single event effects (SEE). Of particular interest are the radiation effects on non-volatile memory devices (NVM). While a major issue relates to the radiation sensitivity of the NVM control circuitry, radiation also affects the performance of the memory cells. At present, the dominant device technology for NVM is based on the floating gate (FG) concept. A promising route for overcoming the technological constraints imposed in device downscaling lies in the use of nanocrystal memories (NC-NVM). Compared to standard FG-NVMs (e.g. Flash EEPROMs), NC-NVMs are expected to show higher tolerance to both TID and SEE effects because of the discrete nature of the charge storage centers.

In this direction, we examined the effect of high-dose proton irradiation on Si-nanocrystal (Si-NC) NVMs (MOS capacitors and nMOS transistors). Irradiation experiments were conducted using protons of 1.5 MeV and 6.5 MeV. The irradiation doses investigated ranged from 1 to 120 Mrad (SiO_2). A 2-D layer of Si NCs with ~3nm mean diameter and 10^{12} cm^{-2} surface density was successfully achieved by low-energy (1 keV) ion-beam-synthesis in thin SiO_2 layers. The final gate dielectric stack includes 6.5nm-thick injection oxide, 2.5nm-thick Si-NC layer and 5nm-thick control oxide. Irradiated devices exhibit a negative threshold-voltage shift compared to non-irradiated samples, in agreement to the well-known observation that irradiation creates a net trapped positive charge (Q_{ot}) into the gate SiO_2 layer. Q_{ot} increases with the irradiation dose and saturates for the high-irradiation regime. No bit flip has been observed on programmed NC-nMOS devices. Charge retention measurements at room temperature for the write and erase states of irradiated and non-irradiated samples reveal that a significant memory window exists at an extrapolated time of ten years even after high irradiation dose. Endurance measurements on irradiated NC nMOS transistors do not show any degradation or drift of the memory window. These preliminary studies suggest that the nanocrystal NVMs may be a attractive route for radiation tolerant electronics.

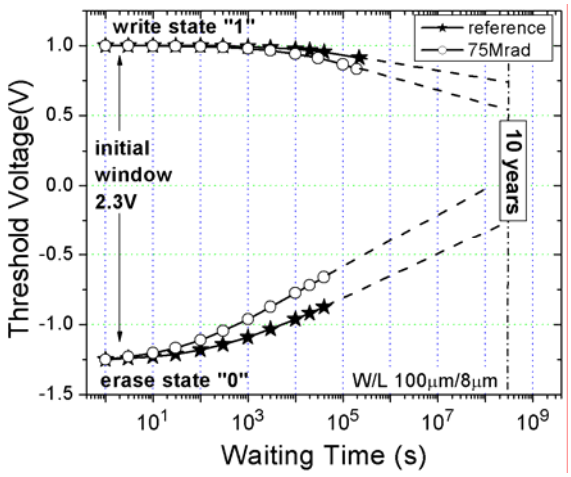

***Fig. II.2.7**. Charge retention characteristics for unirradiated and irradiated NC nMOS transistors at room temperature.*

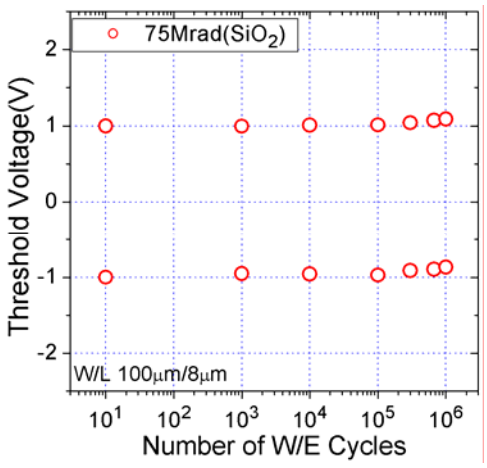

***Fig. II.2.8**. Endurance characteristics of 75Mrad(SiO_2) irradiated NC nMOS transistors tested through 10^6 15ms +9V/-9V write/erase cycles. No degradation or drift in memory window is observed.*

E. Formation of Si nanocrystals in thin SiO_2 layers by plasma-immersion ion-implantation

E. Kapetanakis, P. Dimitrakis, P. Normand

Here, we are concerned with the development of a new Si-NC synthesis route based on plasma-immersion ion-implantation (PIII) in collaboration with CEMES/CNRS and one French SME (Ion Beam Services). Potentially, the PIII technique presents attractive advantages over the conventional low-energy-IBS technique: 1) Access to lower implantation energy that should allow NC fabrication in thinner SiO_2 films; a critical parameter for memory performance. 2) Elimination of energy contamination effects associated with the deceleration mode used in LE-ion implanters; a critical parameter for preserving the integrity of the implanted structures. 3) Ability at providing high ion flux at low energy and therefore, implantation at high doses required for NC formation is possible in reasonable period of time. 4) Finally, the PIII-related instrumentation is relatively simple and thereby, leads at much lower product costs than LE-ion-implanters. Also, PIII is a high throughput technique compatible with conventional CMOS fabrication processes; an important point for further industrial PIII applications.

Our first experiments were conducted using SiF_4 as the plasma gas and 7nm-thick SiO_2 films. Different implantation conditions were tested including Si doses in the 10^{16} – 10^{17} cm^{-2} range and Si energy of 1 and 3.7keV. After post-implantation annealing, the resulting structures were examined by TEM analysis and Al gate MOS capacitor measurement. All in all, our first investigations indicate absence of Si-NCs into the gate oxides as well as significant swelling and dielectric property modification of the implanted matrices. Current work focuses on the use of SiH_4 instead of SiF_4 for avoiding incorporation of high fluorine contents.

PROJECT OUTPUT in 2007

Publications in International Journals

1. “Wet oxidation of nitride layer implanted with low-energy Si ions for improved oxide-nitride-oxide memory stacks”, V. Ioannou-Sougleridis, P. Dimitrakis, V.E. Vamvakas, P. Normand, C. Bonafos, S. Schamm, N. Cherkashin, G. Ben Assayag, M. Perego, M. Fanciulli, Applied Physics Letters 90, 263513 (2007).
2. "Proton radiation tolerance of nanocrystal memories”, E. Verrelli, I. Anastassiadis, D. Tsoukalas, M. Kokkoris, R. Vlastou, P. Dimitrakis, P. Normand, Physica E: Low-Dimensional Systems & Nanostruct. 38, 67-70 (2007).
3. “Parasitic memory effects in shallow-trench-isolated nanocrystal memory devices”, P. Dimitrakis and P. Normand, Solid-State Electronics 51, 125-136 (2007).
4. “Oxide-nitride-oxide memory stacks formed by low-energy Si ion implantation into nitride and wet oxidation”, V. Ioannou-Sougleridis, P. Dimitrakis, V.E. Vamvakas, P. Normand, C. Bonafos, S. Schamm, N. Cherkashin, G. Ben Assayag, M. Perego, M. Fanciulli, Microelectronic Engineering 84, 1986-1989 (2007).
5. "Oxide-nitride-oxide dielectric stacks with Si nanoparticles obtained by low-energy ion beam synthesis”, V. Ioannou-Sougleridis, P. Dimitrakis, V.E. Vamvakas, P. Normand, C. Bonafos, S. Schamm, A. Mouti, G. Ben Assayag, V. Paillard, Nanotechnology 18, 215204 (2007).
6. “Proton radiation effects on nanocrystal non-volatile memories”, E. Verrelli, D. Tsoukalas, M. Kokkoris, R. Vlastou, P. Dimitrakis and P. Normand, IEEE Trans Nuclear Science 54, 975-981 (2007).
7. “Electronic memory device based on a single-layer fluorene-containing organic thin film”, C. Pearson, J.H. Ahn, M.F. Mabrook, D.A. Zeze, M.C. Petty, K.T. Kamtekar, C. Wang, M.R. Bryce, P. Dimitrakis, D. Tsoukalas, Appl. Phys. Lett. 91, 123506 (2007).
8. “Nickel nanoparticle deposition at room temperature for memory applications”, E. Verrelli, D. Tsoukalas, K. Giannakopoulos, D. Kouvatsos, P. Normand, D.E. Ioannou, Microelectronic Engineering 84 (9-10), 1994-1997 (2007).
9. “Electrical properties of metal-oxide-semiconductor structures with low-energy Ge-implanted and annealed thin gate oxides”, E. Kapetanakis, P. Normand, P. Holliger, Journal of Applied Physics, In Press.

Publications in International Conference Proceedings

1. “Oxide-nitride-oxide dielectric stacks with embedded Si-nanoparticles fabricated by low-energy ion-beam-synthesis”, V. Ioannou-Sougleridis, P. Dimitrakis, V. Em. Vamvakas, P. Normand, C. Bonafos, S. Schamm, G. Ben-Assayag, in Materials and Processes for Nonvolatile Memories II, edited by Tingkai Li, Yoshihisa Fujisaki, J.M. Slaughter, Dimitris Tsoukalas, Mater. Res. Soc. Symp. Proc. Volume 997, 0997-I03-1, Warrendale, PA, 2007.
2. “SONOS-type memory structures using thin silicon nitride films modified by low-energy Si+ implantation”, P. Dimitrakis, V. Ioannou-Sougleridis, V. Em.Vamvakas, P. Normand, C. Bonafos, S. Schamm, N. Cherkashin, G. Ben Assayag, M. Perego, M. Fanciulli, Proceedings of 2nd International Conference on Memory Technology and Design 2007, ICMTD 07, pp.213-216, Giens, France, May 7-10, 2007.

Conference Presentations

1. “High-density plasma silicon oxide thin films grown at room-temperature”, M-E. Vlachopoulou, P. Dimitrakis, A. Tserepi, V. Em.Vamvakas, S. Koliopoulou, P. Normand, E. Gogolides, D. Tsoukalas, 29th International Conference on Micro- and Nano-Engineering, MNE 2007, Copenhagen, Denmark, September 23-26, 2007.
2. “Memory and luminescence properties of Si nanocrystals fabricated by ion beam mixing”, V. Beyer, K.-H. Heinig, B. Schmidt, K.-H. Stegemann, P. Dimitrakis, , International Workshop on SEMIconductor NANOstructures 2007 (SEMINANO 2007), Bad Honnef, Germany, June 13-16, 2007.
3. “Microscopy of semiconductor nanocrystals embedded in very thin high k layers by low energy ion-beam-synthesis for memory applications”, C. Bonafos, S. Schamm, P. Dimitrakis, P. Normand, V. Ioannou-Sougleridis, A. Mouti, M. Carrada, A. Slaoui, J. Grob, G. Ben Assayag, B Schmidt, J. Becker, A. Claverie, Microscopy of Semiconducting Mater. XV, P3.009, Churchill College, Cambridge, UK (IOP), April 2-5, 2007.
4. “Oxide-nitride-oxide memory stacks formed by low-energy Si ion implantation into nitride and wet oxidation”, V. Ioannou-Sougleridis, P. Dimitrakis, V.E. Vamvakas, P. Normand, C. Bonafos, S. Schamm, N. Cherkashin, G. Ben Assayag, M. Perego, M. Fanciulli, 15th International Biennial Conference on Insulating Films on Semiconductors, INFOS 2007, Glyfada, Athens, Greece, June 20-23, 2007.
5. “Nickel nanoparticle deposition at room temperature for memory applications”, E. Verrelli, D. Tsoukalas, K. Giannakopoulos, D. Kouvatsos, P. Normand, D.E. Ioannou, 15th International Biennial Conference on Insulating Films on Semiconductors, INFOS 2007, Glyfada, Athens, Greece, June 20-23, 2007.

Conference Organisation

1. 15th International Biennial Conference on Insulating Films on Semiconductors, INFOS 2007, Glyfada, Athens, Greece, June 20-23, 2007 (http://www.infos2007.gr). This conference was organized by the Institute

of Materials Science (IMS) and the Institute of Microelectronics (IMEL) from NCSR Demokritos, the National Technical University of Athens and the University of Ioannina. The 134 papers (119 contributed and 15 invited) presented at the conference are published in A. Dimoulas and P. Normand (Eds), Microelectronic Engineering 84 (9-10), 2007.

Patent

1. Greek Patent Application, No 20070100171, Publication date: 14-03-2007, Method of oxidizing silicon nitride materials at low thermal budgets, Inventors: P. Normand, V. Ioannou-Sougleridis, P. Dimitrakis, V. E. Vamvakas, C. Bonafos, G. Ben Assayag, M. Perego, M. Fanciulli.