Project III. 4: THIN FILM DEVICES for LARGE AREA ELECTRONICS

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Funding

- PENED contract, project code 03ED550, 19/12/2005 – 30/6/2009.

Objectives

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors (TFTs) fabricated in such films. Such advanced TFTs are necessary for next generation large area electronics systems, which are now in the research and development phase. Specifically, the targets of the project are:

- Evaluation of device parameter hot carrier and irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films with sequential lateral solidification (SLS).
- Investigation of the influence of the crystallization technique and the film thickness on TFT performance, defect densities and degradation for technology optimization.
- Investigation of effects of variations in TFT device structure and in the fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Assessment of material properties of ELA poly-Si TFTs using optical measurements.

MAIN RESULTS IN 2008

Task 1: Characterization of SLS ELA TFTs

An easy way to estimate the polysilicon film quality prior to TFT fabrication would be of great importance to the industry. We determined that the difference $V_{g,max}$ - V_{th} (Fig. 1) is a parameter related differently to the poly-Si quality than field-effect mobility μ and threshold voltage V_{th}. It can be used as a new, experimentally obtained, important device parameter characterizing the polysilicon film quality. In Table I the proposed figure of merit $V_{g,max}$ - V_{th} and more typical parameters are shown. We observed much lower μ for TFTs with channels vertical to the boundaries (B vs A and D vs E), as expected, since the grain boundaries reduce μ. However, V_{th} does not seem to be as affected just by the channel orientation (B vs A and D vs E). Other parameters, such as oxide trapped charges and interface charges affect V_{th}. Observing $V_{g,max}$ - V_{th}, we see

that its value is also not as strongly dependent on channel orientation as μ (A vs B). Nevertheless, this parameter does not seem to follow exactly the same behavior as V_{th} (C vs D and D vs E). The previous observations imply that the difference $V_{g,max}$ - V_{th} reflects technological parameters different, or through different relationships, than μ and V_{th}. We probed the physical meaning of $V_{g,max}$ - V_{th} using two approaches, both relating it proportionally to electrically active traps in TFTs. $V_{g,max}$ - V_{th} was then plotted for a double gate TFT (Fig. 2), allowing us to see how it varies with the bottom gate bias V_{gb} and, therefore, what is the effect of V_{gb} on the electrically effective film defects.

TABLE I: DEVICE PARAMETERS

TFT name	Grains vs channel	Field effect mobility μ_{fe} ($cm^2/V\cdot sec$)	V_{th} (V)	$V_{g,max}$-V_{th} (V)
A	⊥	38	0.22	0.48
B	//	145	0.24	0.46
C	//	137	0.53	0.57
D	//	101	0.93	0.57
E	⊥	31	0.94	1.26

To probe the effects of channel doping, both n- and p-channel TFTs fabricated with a novel technique were investigated, oriented along the preferential (X) or the non-preferential (Y) direction. Their degradation mechanisms proved very different, while the channel orientation had a larger effect on n-channel devices than on p- ones (Fig. 3, Fig. 4). To investigate whether the mechanisms are similar for more intense stress, we applied larger stress biases to p-channel devices only. Observing the V_{th} degradation of both X and Y oriented p-channel devices (Fig. 5), we see again very similar behavior for both cases. The stress gate bias being larger, V_{th} degradation is also more intense. The initial electron trapping, implied by the V_{th} increase, has been simulated by others and attributed to a high vertical electric field under the gate, near the drain junction, attracting hot electrons. For large stress times, the trapped negative charges increase the potential barrier. Thus, electron injection tends to saturation, allowing hot hole injection along the whole channel to dominate, causing the subsequent logarithmic V_{th} decrease.

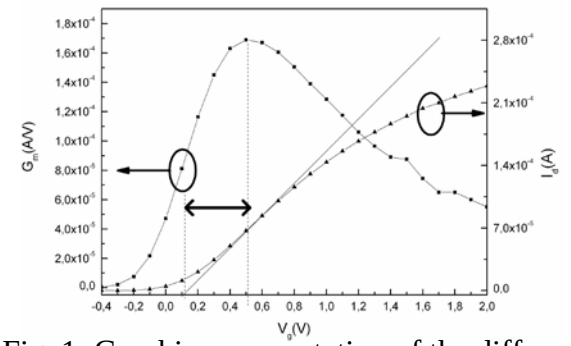

Fig. 1: Graphic representation of the difference of the extrapolated threshold voltage V_{th} and the bias for maximum transconductance $V_{g,max}$.

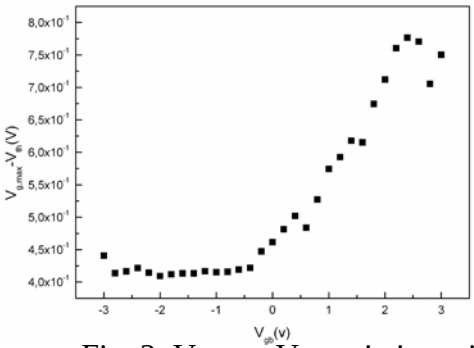

Fig. 2: $V_{g,max}$ - V_{th} variation with bottom gate bias V_{gb} for double gate devices.

The stress intensity, however, seems to affect significantly the μ degradation, since we see a much larger increase for stressing times (Fig. 6). Despite larger degradation, we still do not see any μ decrease. This μ increase has been attributed to a channel shortening effect, due to hot electron injection near the drain. This effect is observed at much larger times, compared to n-channel TFTs, since in these TFTs the spreading of the degraded region along the channel takes longer, due to a lower lateral electric field.

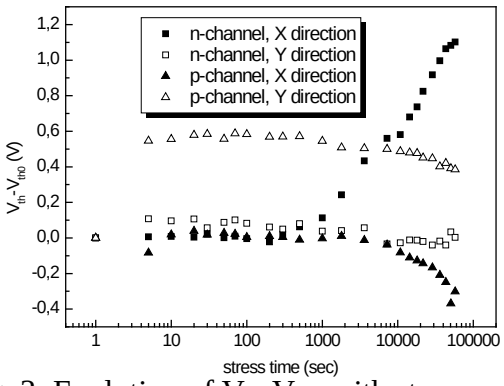

Fig. 3: Evolution of V_{th}-V_{th0} with stress time for both n- and p-channel devices under analogous stress conditions.

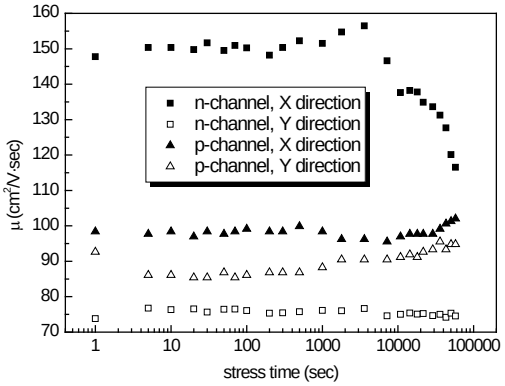

Fig. 4: Evolution of μ with stress time for both n- and p-channel devices under analogous stress conditions.

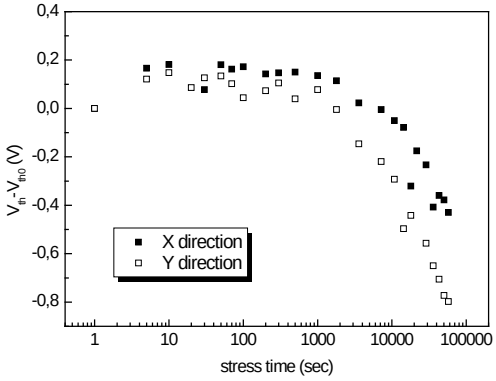

Fig. 5: Evolution of V_{th}-V_{th0} with stress time for p-channel devices under more intense stress.

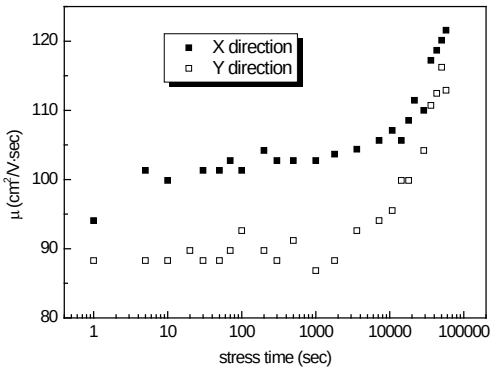

Fig. 6: Evolution of μ with stress time for p-channel devices under more intense stress.

Task 2: Device lifetime investigation under stress

TFTs of different widths W = 2, 8 and 16 μm and of a common length (L = 2 μm) were subjected to different drain biases $V_{DS,stress}$ and gate biases ($V_{GS,stress}$ = around V_{th}, $V_{DS,stress}$ /5, $V_{DS,stress}$ /3 and $V_{DS,stress}$ /2). The on current degradation was examined. The maximum point of degradation of our TFTs was defined to find the magnitude of the degradation as function of $V_{DS,stress}$ and determine their lifetime. Fig. 7 and Fig. 8 show the drain on-current percentage variation for V_{GS} = 5 V and stress time t_{stress} = 660 s.

It was found that the application of a gate bias voltage around the threshold voltage (very low $V_{GS,stress}/V_{DS,stress}$ ratios) becomes the worst hot carrier degradation condition for all the tested devices and for all the applied drain bias voltages $V_{DS,stress}$. Unlike typical bulk MOS transistors, which exhibit their worst degradation behavior when they are submitted to the stress condition $V_{GS,stress} = V_{DS,stress}/2$ (where the substrate current takes its maximum value), the maximum point of on-current degradation in polysilicon TFTs is more frequently observed around the condition $V_{GS,stress} = V_{th}$, especially for high lateral fields. Maximum degradation occurs at $V_{GS,stress} = V_{th}$ because both the electric field near the drain in the channel and the hot electron density are increased. This difference between bulk MOS and poly-Si TFTs mainly derives from the existence of one type of carrier in the channel of poly-Si TFTs, which is intrinsic, whereas both carriers (electron and holes) contribute to bulk MOSFET degradation. However, it was noticed (Fig. 9), for all investigated geometries, that the maximum degradation point progressively shifts towards higher $V_{GS,stress}/V_{DS,stress}$ ratios for lower drain bias voltages.

Fig. 10 shows the variation of on-current measured at V_{GS} = 5 V after each stress cycle for the stress condition yielding the maximum on-current degradation (the worst

degradation performance in each case), for the different drain bias voltages that were applied during stress and for the devices with channel width W = 2 μm. It was noticed that $|\Delta I_{on}/I_{on}|$ exhibited a power-time dependent law of the form: $|\Delta I_{on}/I_{on}| = At^n$ with $n \approx 0.30$-0.36 for all $V_{DS,stress}$ values. This behavior was common for all TFTs with different widths (not shown for W = 8 μm and 16 μm), revealing the same stress degradation mechanism, DAHC (Drain Avalanche Hot Carrier). However, for very intense stress, a saturation law dominated (shown for W = 2 μm and for $V_{DS,stress}$ = 7.5 V and 7.25 V). The pre-power law factor A, that expresses the magnitude of degradation (intensity of hot carrier stress), was found to be also width dependent. So was also the stress parameter b, which is larger for wider devices. Consequently, it was derived that the lifetime to failure for the tested narrower devices in the stress regime $V_{th} \leq V_{GS,stress} \leq V_{DS,stress}/2$ is shorter and narrower TFTs exhibited worse degradation than wider ones.

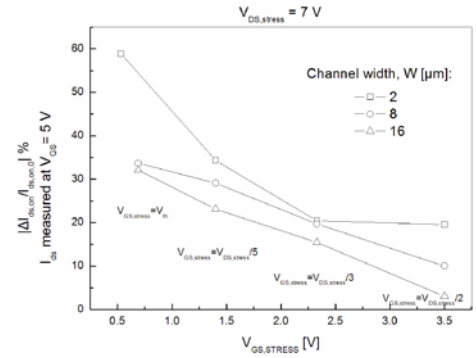

Fig. 7: Relationship between $|\Delta I_{on}/I_{on}|$ % degradation as a function of $V_{GS,stress}$ after 660 s of stress. $V_{DS,stress}$ = 7 V.

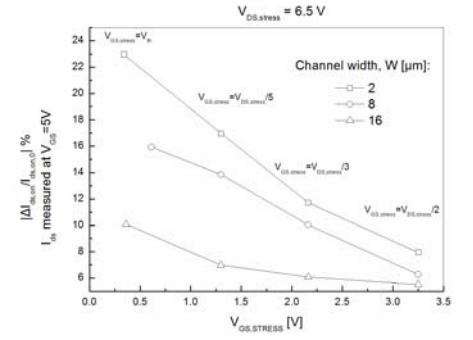

Fig. 8: Relationship between $|\Delta I_{on}/I_{on}|$ % degradation as a function of $V_{GS,stress}$ after 660 s of stress. $V_{DS,stress}$ = 6.5 V.

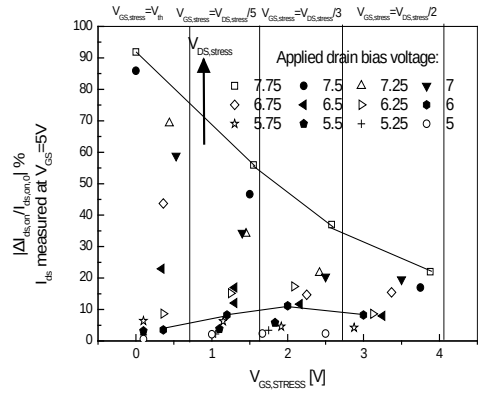

Fig. 9: |ΔIon/Ion| % degradation as a function of $V_{GS,stress}$ and $V_{GS,stress}$ after 660 s of stress. W = 2, L = 2 μm.

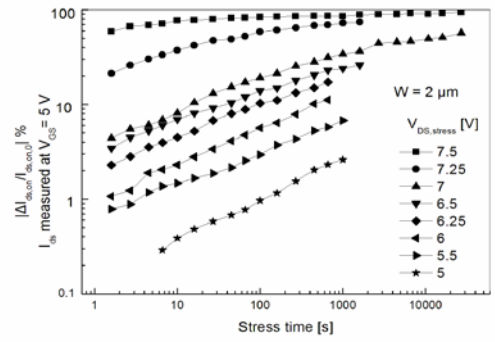

Fig. 10: On drain current % variation measured at V_{GS} = 5 V vs stress duration under various conditions. Parallel shift of the curves is noted. W = 2 μm, L = 2 μm.

Task 3: Investigation of hot carrier stress degradation mechanisms

The relation of the vertical (oxide) field determined by $V_{GS,stress}$ and the lateral field determined by the $V_{DS,stress}$ was investigated to elucidate the degradation mechanisms in the stress regime $V_{th} \leq V_{GS,stress} \leq V_{DS,stress}/2$ and gain insights on improving device hot carrier stress performance. The contribution of the channel width to the degradation was examined for various conditions. To find the origin of the worse degradation performance of narrow width devices the initial normalized stress current was examined; it was noticed that it was more pronounced in narrower devices, i.e. was not

proportional to the ratio of their widths, which means that the magnitude of stress is not normalized over width (Fig. 11). An explanation is the different saturation threshold voltages TFTs with different widths have. Specifically, it has been shown that the DIBL parameter was suppressed as the width is scaled down (Fig. 12). Plotting the V_{th} variation versus the $G_{m,max}$ percentage change (Fig. 13), we noticed that when V_{th} variation became prominent, the percentage $G_{m,max}$ change was above 15-20%, which implies that: i) the V_{th} variation is apparent and is attributed to the contribution of $G_{m,max}$ to V_{th}, not originating by a significant carrier trapping mechanism, ii) the degraded region in narrow devices is formed faster.

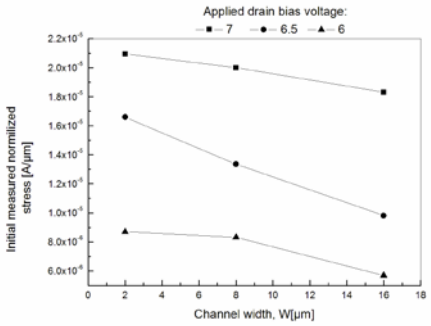

Fig. 11: Normalized (over width) value of initial drain stress current vs. channel width (W = 2, 8 and 16 μm). Conditions: $V_{GS,stress} = V_{th}$, $V_{DS,stress}$ = 6, 6.5, 7 V.

Further, the width dependent degradation was examined for $V_{GS,stress} = V_{DS,stress}$.

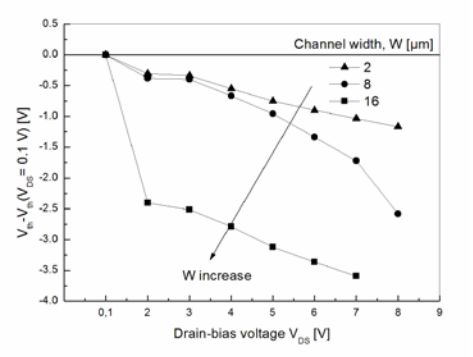

Fig. 12: Difference of V_{th} at saturation as compared to V_{th} in the linear regime for various drain biases for TFTs with different widths (W = 2, 8 and 16 μm).

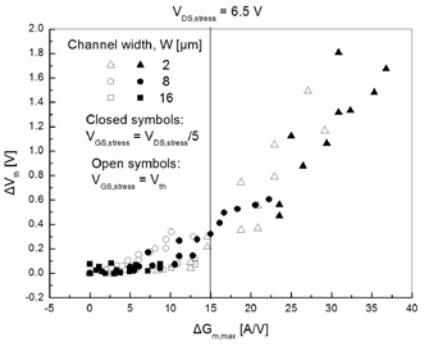

Fig. 13: V_{th} change vs $G_{m,max}$ % variation for 3 widths. $V_{GS,stress} = V_{th}$, $V_{DS,stress}/5$ for $V_{DS,stress}$ = 6.5 V. Points beyond the line are closer to the hottest carrier condition.

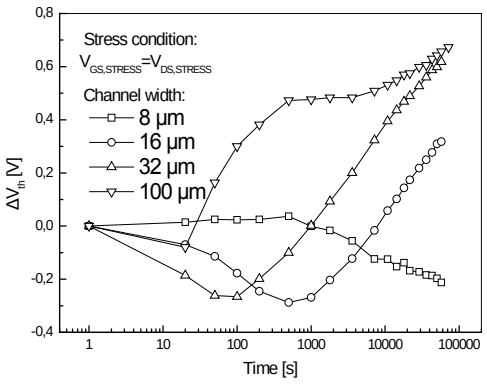

Fig. 14: V_{th} variation during stress for Y-directed TFTs with various widths. $V_{GS,stress} = V_{DS,stress}$ = 4.8 V.

The tested TFTs had various widths (W = 8, 16, 32, 100 μm) and a common length (L = 0.8 μm). For wide channel devices we observed a larger parallel shift of the transfer characteristics during stress, even in the subthreshold region. We also noted that the stressing time at which each TFT exhibited the positive ΔV_{th} onset occurred earlier for wider devices (Fig. 14). Moreover, we observed an initial ΔV_{th} decrease with stress time, and then an increase, a common behavior in all devices. A larger decrease of V_{th} for TFTs with W = 100 μm was found; TFTs with W = 8 μm did not reach the time point at which ΔV_{th} exhibited the positive onset, for the stress durations used. With further stress, the ΔV_{th} vs. stress duration curve was width independent and all devices exhibited the same behavior of a continuous ΔV_{th} increase with the same slope. This width dependent degradation behavior was also seen in the subthreshold slope.

We proposed a new mechanism to expain the difference in degradation behavior between narrow and wider TFTs. According to it, a width-depended thermal energy source is provided by the self-heating effects (more pronounced for high gate biases, because the current is larger) to the positive mobile ions in the SiO_2 film. Because the heating was higher for wider TFTs (more pronounced self heating effects), the condition of electron injection was satisfied earlier; thus, electron injection changed the direction of V_{th} shift earlier. In addition, the V_{th} negative shift reached a maximum value that depended on temperature, mobile ion density and applied field, approximately the same for all TFTs. Eventually, the typical CHE injection mechanism for $V_{GS,stress} = V_{DS,stress}$ dominated and overwhelmed the initial negative voltage shift.

Task 4: Low temperature and transient current characterization

TFT characterization was performed at 100 K to 450 K for the investigation of thermally activated mechanisms; these measurements and trap state density estimations were carried out at the University of Athens, in a project collaboration. It was found that the activation energies for all parameters become larger as the film thickness is reduced. In thicker films generation takes place mainly through deeper states; in thinner films tail states, introduced by lack of periodicity due to grain boundaries, more frequent in thinner films, are significant. Overshoot and undershoot transient drain currents were investigated and correlated with the thermally generated mechanisms, to extract information on carrier generation and capture processes in SLS ELA polysilicon films.

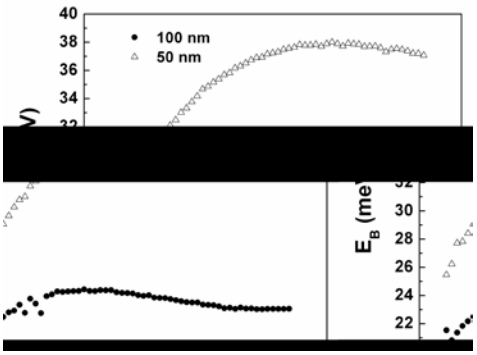

Fig. 15: Temperature dependence of the grain boundary barrier height for TFTs in 50 nm and 100 nm polysilicon films.

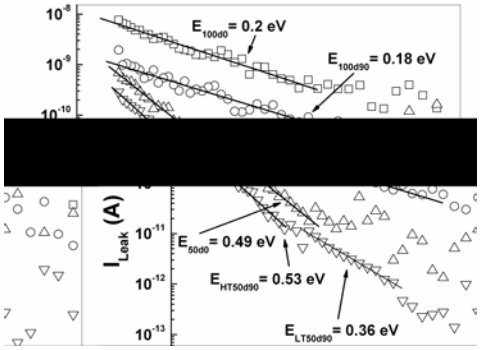

Fig. 16: Leakage current activation energies for X-oriented (0°) and Y-oriented (90°) TFTs in 50 nm and 100 nm polysilicon films.

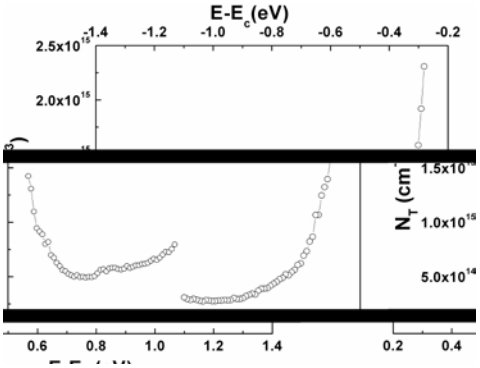

Fig. 17: Estimated trap density (separately calculated in each half of the band gap using DLTS measurements) in the silicon band gap for n-channel TFTs fabricated in 30 nm SLS ELA polysilicon films.

The temperature dependence of the grain boundary barrier height was estimated, comparing measurements for X-oriented vs. Y-oriented TFTs, as shown in Fig. 15. Activation energy E_a values for the leakage current I_{leak} were found to be similar for X-oriented and Y-oriented TFTs, as observed in Fig. 16, indicating that the responsible generation mechanism refers not just to grain boundaries but to intragrain material properties. Moreover, the thermally activated generation mechanisms were related with

the gap states; a methodology was developed for the determination of the temperature dependence of the grain boundary potential barriers and of the trap density in the silicon energy gap. The estimated trap density in the silicon band gap is shown in Fig. 17.

Task 5: Material / optical characterization

During 2008, we continued our research on the optical properties of our advanced SLS ELA poly-Si films, a field where little documentation exists, at the moment. Proceeding to the film analysis through spectroscopic ellipsometry measurements, we examined the Ψ parameter in respect to wavelength and attempted fitting of these experimental data using the 4-oscillator Forouhi-Bloomer model to describe the film refractive index. The fitting of the experimental curves with the aforementioned model proved very good. A typical example of the experimental data acquired and the resulting fitting can be seen in Fig. 18. We followed the same fitting procedure for all of the SLS ELA samples, but also for amorphous Si (a:Si) and crystalline Si (c-Si) as references. All SLS-ELA films showed similar behavior with respect to their optical properties, however, that was very different from the cases of a:Si and c-Si.

Having observed this differentiation of SLS ELA optical properties from a:Si and c-Si, we proceeded with XRD measurements of our films, to further probe the nature of the polysilicon we examined. In Fig. 19, we can see the obtained XRD spectra for all three SLS ELA films. As we see, all of the films again show similar behavior, with the prevailing peak angle being at around 21.5°. This angle corresponds to a Si modification named allo-Si, according to literature. The above data indicate that SLS-ELA Si films may possibly have a crystallographic structure similar to that of the so-called allo-Si.

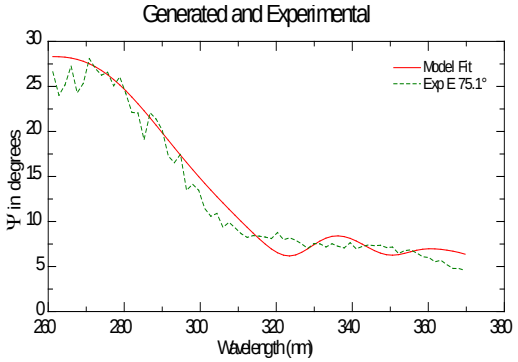

Fig. 18: Fitting of the spectroscopic ellipsometry obtained Ψ parameter, utilizing the Forouhi-Bloomer model, for an advanced SLS ELA thin film.

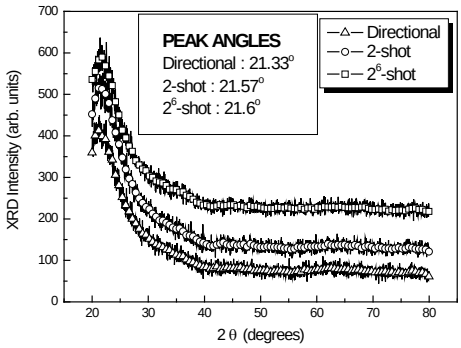

Fig. 19: XRD spectra for the three differently crystallized SLS ELA polysilicon films.

PROJECT OUTPUT IN 2008

1. Publications in International Journals and Reviews

1. Moschou, D.C., M.A. Exarchos, D.N. Kouvatsos, G.J. Papaioannou, A. Arapoyanni and A.T. Voutsas, "Reliability and defectivity comparison of n- and p-channel SLS ELA polysilicon TFTs fabricated with a novel crystallization technique", Microelectronics Reliability 48 (8-9), 1544, August-September 2008.
2. Moschou, D.C., M.A. Exarchos, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, "A novel SLS ELA crystallization process and its effects on polysilicon film defectivity and TFT performance", Microelectronic Engineering 85 (5-6), 1447, May-June 2008.
3. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos, F.V. Farmakis and A.T. Voutsas, "Characterization of thin film transistors fabricated on different sequential lateral

solidified poly-silicon substrates", Microelectronic Engineering 85 (5-6), 976, May-June 2008.

4. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "Investigation of the undershoot effect in polycrystalline silicon thin film transistors", Solid State Electronics 52 (3), 394, March 2008.
5. Kontogiannopoulos, G.P., F.V. Farmakis, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, "Hot carrier stress induced degradation of SLS ELA polysilicon TFTs – Effects of gate width variation and device orientation", Solid State Electronics 52 (3), 388, March 2008.
6. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "Role of band gap states on the electrical behaviour of sequential lateral solidified polycrystalline silicon TFTs", Journal of the Electrochemical Society 155 (1), H1, January 2008.

2. Publications in Conference Proceedings

7. Verrelli, E., D. Tsoukalas and D. Kouvatsos, "Deposition and electrical characterization of hafnium oxide films on silicon", Physica Status Solidi (c) 5 (12), 3720, December 2008.
8. Exarchos, M.A., D.C. Moschou, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "Performance of thin-film transistors fabricated by sequential lateral solidification crystallization techniques", Physica Status Solidi (c) 5 (12), 3634, December 2008.
9. Moschou, D.C., G.P. Kontogiannopoulos, D.N. Kouvatsos and A.T. Voutsas, "The effect of crystallization technology and gate insulator deposition method on the performance and reliability of polysilicon TFTs", Physica Status Solidi (c) 5 (12), 3630, December 2008.
10. Moschou, D.C., E. Verrelli, D.N. Kouvatsos, P. Normand, D. Tsoukalas, A. Speliotis, P. Bayiati and D. Niarchos, "Investigation of top gate electrode options for high-k gate dielectric MOS capacitors", Physica Status Solidi (c) 5 (12), 3626, December 2008.
11. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "An experimental study of band gap states electrical properties in poly-Si TFTs by the analysis of the transient durrents", Physica Status Solidi (c) 5 (12), 3613, December 2008.
12. Kontogiannopoulos, G.P., F.V. Farmakis, D.N. Kouvatsos, G.J. Papaioannou and A.T. Voutsas, "Width dependent degradation of polycrystalline silicon TFTs", Proceedings of the 26th International IEEE Conference on Microelectronics (MIEL 2008), p. 549, Nis, Yugoslavia, May 2008.

3. International Conference Presentations

13. Moschou, D.C., M.A. Exarchos, D.N. Kouvatsos, G.J. Papaioannou, A. Arapoyanni and A.T. Voutsas, "Reliability and defectivity comparison of n- and p-channel SLS ELA polysilicon TFTs fabricated with a novel crystallization technique", 19th European Symposium - Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2008), Maastricht, The Netherlands, October 2008.
14. Exarchos, M.A., G.J. Papaioannou, D.C. Moschou, D.N. Kouvatsos, A. Arapoyanni and A.T. Voutsas, "On the study of p-channel Thin-Film Transistors fabricated by SLS ELA crystallization techniques", European Materials Research Society Spring 2008 Meeting, Symposium I: Thin Film Materials for Large Area Electronics, Strasbourg, France, May 2008.
15. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "Back gate influence on front channel operation of p-channel double gate polysilicon TFTs", European Materials Research Society Spring 2008 Meeting, Symposium I: Thin Film Materials for Large Area Electronics, Strasbourg, France, May 2008.