## Project II.2: MATERIALS AND DEVICES FOR MEMORY APPLICATIONS

**Project leader: P.Normand**
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**Collaborating Researchers**: P. Argitis, N. Glezos, A.M. Douvas
**Post-doctorals**: E. Kapetanakis*, E. Makarona, D. Velessiotis
**PhD candidate**: P. Goupidenis
**From June 2008: Assistant Professor at the Department of Electronics, TEI Crete*

### Objectives

- Development of functional dielectrics and nanostructured materials for inorganic/organic memory applications.
- Study of the structural and electrical properties of the generated materials and demonstration of material functionality enabling the development of low-voltage memory devices.
- Realization and testing of memory devices and manufacturability assessment of the developed fabrication routes in an industrial environment.

### Funding

- Bilateral French-Greek Project, Si-Nanocrystal Synthesis by Plasma-Immersion Ion-Implantation for Non-Volatile Memory Applications, EPAN. M.4.3.6.1E.
- III-Nitrides quantum dots-resonant tunneling diodes as tunable wavelength UV-VIS phototodetectors, European Space Agency (ESA), RFQ No. 3-12083

### Activities

Our research activities in materials and structures for memory applications started in 1996 with the development of the low-energy ion-beam-synthesis (LE-IBS) technique in collaboration with Salford University (UK). Two-dimensional arrays of Si nanocrystals in thin gate dielectrics were demonstrated and further exploited in the fabrication of nanocrystal memories (NCMs). This activity was first supported by the EU project, FASEM (1997-2000). LE-IBS development with target the realization of non-volatile NCMs in an industrial environment has been conducted further within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer, Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last few years to novel NCMs alternatives including: (a) Memory devices by $Si^+$ irradiation through poly-Si/$SiO_2$ gate stack (Collaborators –CLRs-: FZR and ZMD AG both sited in Dresden (DE)), (b) Memory devices using Ge-NCs produced by MBE (CLR: Aarhus Univ. (DK)), (c) hybrid silicon-organic and SiGe-organic memories (CLR: Durham Univ. (UK)); this last activity was conducted within the framework of the EU project, FRACTURE (2001-2003), (d) formation of LE-IBS Ge-NCs in high-k dielectrics (CLRs: CEMES/CNRS (FR), FZR Dresden and Cambridge NanoTech (USA)), (e) Formation of Si NCs in thin $SiO_2$ layers by Plasma Immersion (CLRs: CEMES/CNRS & Ion-Beam-Services (IBS, FR)), (f) Wet oxidation of silicon nitride implanted with low-energy Si ions for ONO memory stacks (CLRs: CEMES/CNRS and MDM-INFM (IT)), (g) MOS structures with low-energy Ge-implanted thin gate oxides (CLR: LETI/CEA (FR)), (h) Proton radiation tolerance of nanocrystal memories (CLR: NTUA (GR)), (i) Fabrication and characterization of SiO2 films with Si NCs obtained by stencil-masked LE-IBS (CLR: CEMES/CNRS and INSA Toulouse (FR)).

In 2008, our main activities focused on the following tasks: (A) Molecular storage elements for proton memory devices (CLRs: IMEL's projects I.2 & II.3), (B) Fluorene-based cross-bar organic memory device (CLRs: NTUA and Durham Univ.), (C) High-k dielectrics stacks for advanced non-volatile memory devices (CLRs: Helsinki Univ. (FI) & IMS/NCSR'D' (GR)), (D) III-Nitrides quantum dots-resonant tunneling diodes as tunable wavelength UV-VIS phototodetectors (CLR: MRG/FORTH (GR)), (E) Fabrication and characterization of Ge diodes (CLR: IMS/NCSR'D').

## A. Molecular storage elements for proton memory devices

**E. Kapetanakis, A.M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Normand**

With the increasing challenge in flash memory scaling, various information storage elements based on novel gate materials and physical storage principles have been proposed. Significant efforts have been devoted to storage elements exploiting: a) charge injection and trapping in dielectrics or nanoparticles, ferroelectric polarization of dielectrics, and c) the motion and trapping of protons in dielectrics (proton memory).

Apart from the benefits of using a single-transistor memory architecture and of being radiation tolerant, the proton memories also have the advantage of being able to be programmed at very low voltages, thus offering an attractive alternative for low-power low-voltage non-volatile data storage. While promising device results have been obtained, the conventional methods of forming proton memories still face critical issues towards the development of commercial products. For example, all existing methods utilize proton generating techniques (high-temperature processing and ion implantation) that can seriously affect the logic structures on the chip and cannot control the number of generated protons, thereby introducing large variations in device-to-device performance. In addition, the current fabrication methods of proton memory devices are not compatible with the emerging memory technologies of “all-polymer” ICs. Therefore, it is highly desirable to find a simple and low-cost method able to produce proton-based storage elements that can be reliably incorporated into the gate of inorganic and/or organic transistors.

Towards this goal, we recently reported the use of storage elements based on mobile protons that naturally exist in a solution-processed proton-conducting polymeric material. Such an approach does not involve a processing step for introducing protons inside the storage element, a trait that reduces complexity and cost in device fabrication. Moreover, a solution-based fabrication method can offer the capability for manipulating the storage elements’ properties simply via formulation of the solution or/and chemical synthesis; a feature which is necessary for the modulation and optimization of the device overall memory performance. In addition, solution-processed elements provide compatibility with mechanically flexible substrates, low-cost manufacturing and large-area integration, and thereby, may be exploited for producing “all-polymer” single-transistor memories.

Realization of non-volatile memory devices is achieved using a stacked structure consisted of a proton-conducting polymeric layer (PCL) based on a tungsten heteropolyacid and poly(methyl methacrylate) (PMMA), and a proton-trapping polymeric layer (PTL) based on PMMA containing amine proton trapping sites, as depicted in figure 1 in the case of a MIS-type capacitor. Application of a positive voltage to the gate electrode with the substrate connected to ground (“Write” operation) allows for the dissociation of neutral (n) sites of the PCL into anions (-) and protons (+), motion and trapping of protons in the PTL. This induces a negative flat-band voltage shift of the capacitor C-V characteristics. A subsequent negative voltage moves back the trapped protons leading to the reformation of neutral sites within the PCL (“Erase” operation).

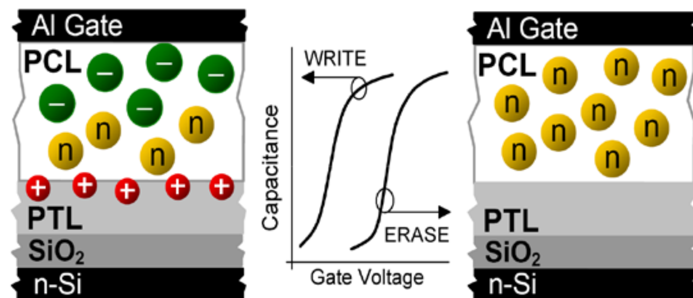


**Figure 1:** Schematic illustrating the structure and the operation principle of a non-volatile bistable MIS memory device with a molecular-based proton storage element consisting of a proton-conducting polymeric layer (PCL) and a proton-trapping polymeric layer (PTL) bi-layer stacked structure.

## B. Fluorene-based cross-bar organic memory device

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***Centre for Molecular and Nanoscale Electronics, Durham University (UK)*

Organic and polymer materials are promising candidates for future molecular-scale electronic applications. Their attractive features include good processability, scalability and the possibility for molecular design through chemical synthesis. As an emerging area in organic electronics, polymer memories have become an active research topic in recent years. They are likely to be a promising alternative to the conventional memory technologies facing the challenges in miniaturizing from microscale to nanoscale. The last two decades various memory concepts and molecular materials have been examined with particular emphasis on the metal/organic/metal bistable two terminal devices. For such devices, application of appropriate voltage pulses switches the resistance of the organic material from a high state to a low state and vice versa. Each resistance state corresponds to a memory state or in other words represents a bit of information. A stringent challenge is here to synthesize an organic material exhibiting resistance switching using unipolar pulses.

In this context, our group in collaboration with Durham University focused on molecules containing the fluorene-group. We previously demonstrated (APL, 91(2007), 123506) that 7-{4-[5-(4-*tert*-butylphenyl)-1,3,4-oxadiazol-2-yl]phenyl}-9,9-dihexyl-*N*,*N*-diphenyl-fluoren-2-amine exhibit switching and negative differential resistance (NDR) measurements. Further, we examined the switching and NDR mechanisms and how the top-metal layer (Al) formation conditions affect the device operation. For these studies two different measurement protocols have been developed based on I-V measurements utilizing (1) single-directional voltage sweep and (2) bi-directional voltage sweep in combination with high and low electrode reversing. In most cases, a “forming” process, in which a large positive voltage is applied to the top Al electrode, was required before the NDR and resistance switching be observed. Three different electrical conductivity regimes have been identified: Poole–Frenkel conductivity in unformed structures, linear I-V characteristics for the low resistance state in formed devices, and superlinear I-V behavior for the high resistance state in formed devices.

Models based on metallic filaments or on the injection and storage of charge cannot explain all our experimental observations. Instead, our results suggest the formation of nanocrystalline regions that locally modify the polymer film resistivity. In addition, we found that polymer+0.5% of Au nanoparticles blends improve the switching phenomena and enhance device reliability. The devices can be used as two-terminal memory cells operating with unipolar voltage pulses in the regime of 1s. Low resistivity state can be achieved utilizing +3V pulses (i.e., peak voltage of the NDR region) on top-electrode independently on the thickness of the organic layer (Fig.2). High resistivity state is achieved using +5V, +6V and +8V (i.e., valley voltage of the NDR region) for devices with layers 40nm, 50nm and 70nm respectively (Fig.3). The current difference at a certain voltage between these states defines the memory window which is around two orders of magnitude.

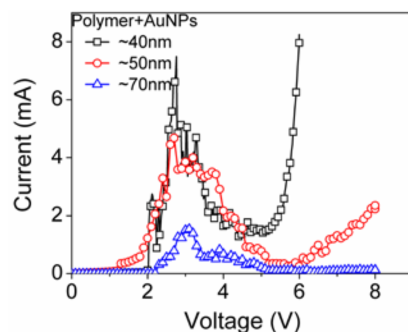


**Fig.2**: I-V characteristics exhibiting strong NDR regions for different organic layer thicknesses

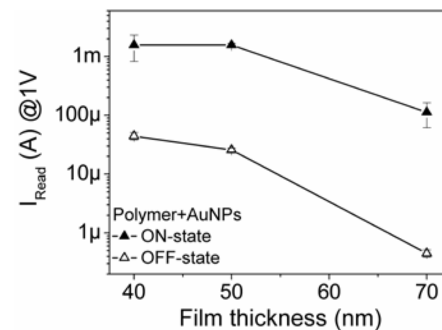


**Fig.3**: Current level differences between the low (ON) and the high (OFF) resistivity states as function of organic layer thickness.

## C. High-k dielectrics stacks for advanced non-volatile memory devices

**V. Ioannou-Sougleridis, P. Dimitrakis, P. Normand, K. Kukli*, J. Niinisto*, M. Ritala*, M. Leskela***
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The overall objective of this project is to explore advanced atomic-layer-deposition (ALD) precursor chemistry of high-k dielectrics used as tunnel or control insulators of nitride-based memory structures in order to improve the functionality and performance of SONOS-type devices. This project is conducted in close collaboration with the University of Helsinki.

Silicon nitride memory technology has significant advantages that could alleviate the scaling restrictions of the conventional flash technology. Silicon nitride technology employs ONO (oxide-nitride-oxide) dielectric stacks and utilizes traps that exist in the nitride layer as individual charge storage nodes. Despite the inherent advantages of the nitride technology it suffers from a number of drawbacks with most important the notorious “erase-saturation” effect. These problems can be bypassed using a number of approaches that include the replacement of the control and bottom oxides by single or multi-layer dielectric stacks composed of high-k insulators and also the replacement of the polysilicon gate electrode by a high work function metal electrode. These modifications provide a material based engineering solution of the erase-saturation effect. The use of high-k insulators increases the total EOT of the structure, allowing the use of a thicker control oxide. Additionally, the use of such dielectric stacks provides a significant number of parameters such as energy gaps, band offsets, dielectric constants and thicknesses of the stack layers, as well as stack layer ordering (i.e. low-k/high-k or high-k/low-k) that under proper consideration may lead to advanced and scalable non-volatile memory cells.

ALD precursor chemistry is becomes gradually the critical factor which determines the physical, chemical and electrical properties of the deposited high-k insulators. This year we examined $Al_2O_3$, $HfO_2$ and $ZrO_2$ materials synthesized by different precursor chemistries such as $Al(CH_3)_3$-$H_2O$, ($Al_2O_3$), $Zr[N(C_2H_5)(CH_3)]_4$-$O_3$, ($ZrO_2$), $(CpMe)_2Zr(OMe)Me$-$O_3$, ($ZrO_2$), $Hf[N(C_2H_5)(CH_3)]4$-$O_3$, ($HfO_2$) and $(CpMe)_2Hf(OMe)Me$-$O_3$ ($HfO_{2)}$. These materials were evaluated through structural studies and electrical characterization of oxide-nitride-high-k dielectrics stacks. Fig.4a shows the charging characteristics (flat-band voltage shift) of the as-grown oxide-nitride–$ZrO_2$ ($Zr[N(C_2H_5)(CH_3)]_4$-$O_3$) dielectric stack after consecutive pulses of 100 ms, and Fig. 4b shows the dynamic response of the same dielectric stack under varying height write-erase pulses.

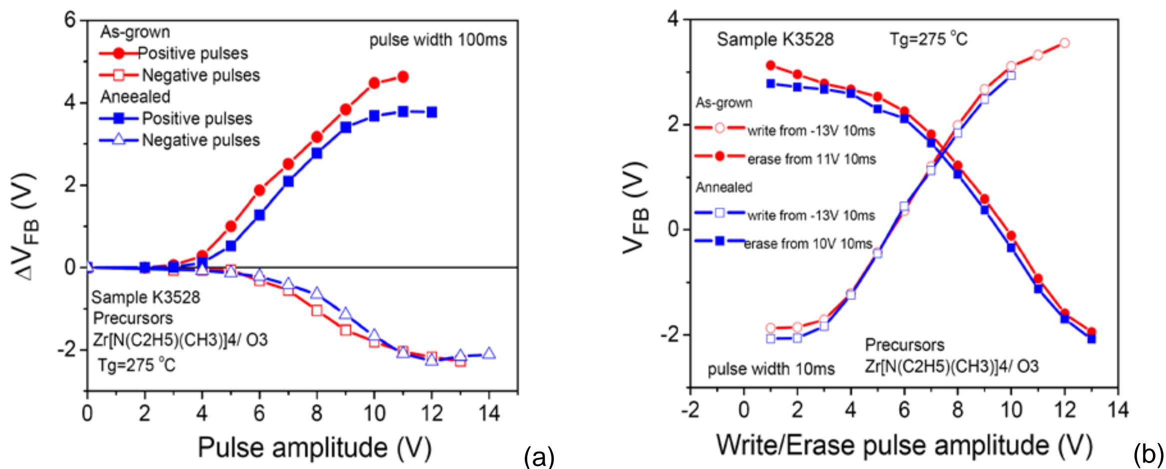


**Fig.4**: Write/Erase characteristics of Oxide-Nitride-$ZrO_2$ stacks. (a) Flat-band voltage shift as a function of the 100ms applied pulse amplitude and (b) flat-band voltage as a function of 10ms write/erase pulses for 10ms/-13V and 10ms/11V starting memory states.

## D. III-Nitrides quantum dots-resonant tunneling diodes as tunable wavelength UV-VIS phototodetectors

**P. Dimitrakis, E. Iliopoulos*, G. Deligiorgis*, P. Normand, G. Konstantinidis*, A. Georgakilas***
**Department of Physics & MRG/FORTH (GR)*

The objective of these activities is to design, fabricate and evaluate the performance of a novel solid-state photodetector device with spectroscopic capability, operating in the ultraviolet-visible part of the electromagnetic spectrum. The proposed device principle combines the broad spectrum responsivity of a layer containing non-uniform size distribution of (In)GaN quantum dots (QDs) with energy selective read-out mechanism based on AlGaN/GaN asymmetric double quantum-well resonant tunneling diode (RTD) structure (Fig.5).

Theoretical modeling (MRG/FORTH) of the structure was first realized allowing for the calculation of the RTD tuning range as a function of the composition of the quantum-wells (QWs), i.e., the AlN mole fraction. The effect of the geometrical characteristics of the NPs and their density were taken into account for the calculation of the RTD tuning range. Meanwhile, self-consistent calculations of the Schrodinger-Poisson equations considering analytical expressions for the calculation of piezoelectric fields were performed using the code developed by MRG allowing for the precise estimation of the energy band diagram under different external applied bias conditions. Towards, the development of insulating dielectric materials of the proposed structures, IMEL provided TEOS layers deposited by LPCVD and characterized different layers (e.g. PE-CVD SiN) and processes. After dielectric optimization, MRG fabricated RTD structures of various configurations (e.g. single-well, double-well, various thicknesses of the layers, various AlN mole fractions) which are under testing at IMEL. Typical I-V curves of the fabricated diodes exhibiting a clear NDR region are reported in figure 6. The hysteresis behavior detected after forward and backward voltage sweeps is probably due to the charge trapping that occurs at the lateral surface of the vertical multilayer stack of the diode in combination with the presence of strong piezoelectric fields. This undesirable hysteresis effect was also reported by other groups and its elimination constitutes a difficult task to overcome.

In addition, different MBE growth conditions have been tested to examine the growth mechanisms of the GaN QDs. Comprehensive AFM studies reveal that the required height-to-diameter ratio for our application can be achieved by applying a two-step growth process. In order to investigate the electrical properties of the QDs, special diode structures have been fabricated and tested using C-V and I-V measurements. Finally, according to the device architecture, the top electrode should be a transparent electrode. Different transparent metal oxide conductors (e.g. ITO) are under investigation at IMEL in collaboration with the IMS/NCSR'D' (A. Speliotis).

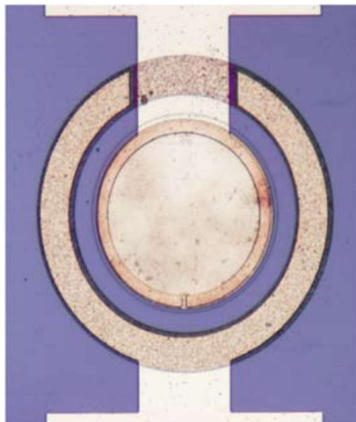

**Fig. 5:** Optical Microscope image of a 100μm diameter two-terminal diode.

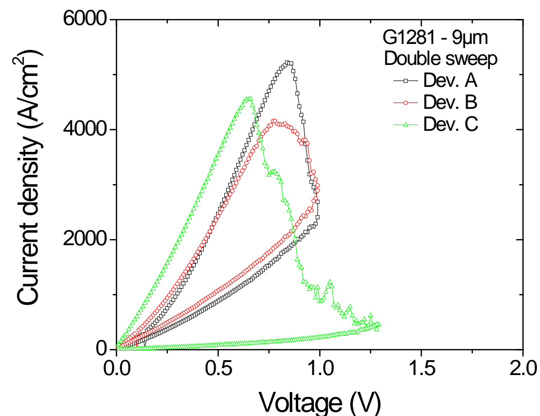


**Fig. 6:** I-V characteristics of three different RTD diodes exhibiting hysteresis

### E. Fabrication and characterization of Ge diodes

**V. Ioannou-Sougleridis, P. Dimitrakis, P. Normand, A. Speliotis*, A. Dimoulas***
**Institute of Materials Science NCSR 'D'*

The objective of this research activity is the fabrication and assessment of junction diodes on Ge substrates. Germanium was recently suggested as an alternative substrate that could alleviate the significant scaling limitations of the conventional Si MOSFET. Ge has a number of attractive properties which may lead to the development of nanoscale transistor structures. The lower effective masses and the resulting higher mobility of both type of charge carriers (two times higher than Si for electrons and four times for holes) in Ge, makes this material ideally suited as channel material for high-performance logic applications. However, the substitution of silicon by Ge substrates is not technological a straightforward task. The study will examine the dependence of the diode electrical characteristics (such as the reverse current, ideality factor and surface states effects) upon the main fabrication parameters (implantation and annealing) and the different surface passivation materials such as GeOx, Si/HfO2, La2O3,/HfO2, GeO2/HfO2, GeOx/HfO2, GeOx/ZrO2. This activity takes place in collaboration with the Institute of Materials Science NCSR "D" within the framework of FP7-ICT project DUALLOGIC.

## PROJECT OUTPUT in 2009

### Publications in International Journals

1. "Molecular storage elements for proton memory devices", E. Kapetanakis, A.M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Normand, Advanced Materials 20, 4568-4574 (2008).
2. "Electrical behavior of memory devices based on fluorene-containing organic thin films", P. Dimitrakis, P. Normand, D. Tsoukalas, C. Pearson, J.H. Ahn, M.F. Mabrook, D.A. Zeze, M.C. Petty, K.T. Kamtekar, C. Wang, M.R. Bryce, M. Green, Journal of Applied Physics 104, art. no. 044510 (2008).
3. "KFM detection of charges injected by AFM into a thin SiO2 layer containing Si nanocrystals", C. Dumas, L. Ressier, J. Grisolia, A. Arbouet, V. Paillard, G. BenAssayag, S. Schamm, P. Normand, Microelectronic Engineering 85, 2358-2361 (2008).
4. "Electrical properties of metal-oxide-semiconductor structures with low-energy Ge-implanted and annealed thin gate oxides", E. Kapetanakis, P. Normand, P. Holliger, Journal of Applied Physics 103, art. no. 064515 (2008).
5. "Study of charge storage characteristics of memory devices embedded with metallic nanoparticles", Ch. Sargentis, K. Giannakopoulos, A. Travlos, P. Normand, D. Tsamakis, Superlattices and Microstructures 44, 483-488 (2008).
6. "Silicon nanoparticles synthesized in SiO2 pockets by stencil-masked low energy ion implantation and thermal annealing", J. Grisolia, C. Dumas, G. Ben Assayag, C. Bonafos, S. Schamm, A. Arbouet, V. Paillard, M.A.F. van den Boogaart, J. Brugger, P. Normand, Superlattices and Microstructures 44, 395-401 (2008).
7. "High-density plasma silicon oxide thin films grown at room-temperature", M.E. Vlachopoulou, P. Dimitrakis, A. Tserepi, V.Em. Vamvakas, V.Em., S. Koliopoulou, P. Normand, E. Gogolides, D. Tsoukalas, Microelectronic Engineering 85, 1245-1247 (2008).

### Publications in International Conference Proceedings

1. "Low-energy ion-beam-synthesis of semiconductor nanocrystals in very thin high-k layers for memory applications", C Bonafos, S Schamm, A Mouti, P Dimitrakis, V Ioannou-Sougleridis, G Ben Assayag, B Schmidt, J Becker, P Normand, in Microscopy of Semiconducting Materials 2007, A. G. Cullis and P. A. Midgley Editors, Springer Proceedings in Physics V.120, 321-324 (2008).

2. D.C. Moschou, E. Verrelli, D.N. Kouvatsos, P. Normand, D. Tsoukalas, A. Speliotis, P. Bayiati, D. Niarchos, Investigation of top gate electrode options for high-k gate dielectric MOS capacitors, Physica Status Solidi (C) 5, 3626-3629 (2008).

### Chapter in Book

1. "Silicon nanocrystal memories", P. Dimitrakis, P. Normand, D. Tsoukalas, in Silicon Nanophotonics, L. Khriachtchev Editor, Pan Stanford Publishing, Chap. 8, 211-244, 2008.

### Conference Presentations

1. "Hybrid organic-inorganic materials for molecular proton memory", E. Kapetanakis, A. M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Normand, Presented at: 34th International Conference on Micro- and Nano-Engineering, MNE 2008, Athens, Greece, September 15-19, 2008.
2. "Nanostructured ZnO-based layers deposited by non reactive rf magnetron sputtering on ultra-thin SiO2/Si through a stencil mask", A. Barnabé, M. Lalanne, L. Presmanes, Ph. Tailhades, C. Dumas, J. Grisolia, M. Naceur, A. Arbouet, V. Paillard, G. BenAssayag, M.A.F. van den Boogaart, J. Brugger, P. Normand, Presented at: 2nd International Symposium on Transparent Conductive Oxides, Hersonissos, Crete, Greece, October 22-26 2008.,
3. "Self-organization of Cu nanoparticles on polythiophene layers for bistable memory devices", P. Dimitrakis, M. Vassilopoulou, L.C. Palilis, G.Papadimitropoulos, D. Davazoglou, P. Argitis, P. Normand, E-MRS 2008 Spring Meeting, Symposium Q, Strasbourg, France, June 2008.

### Invited Talks

1. "Des alternatives pour les mémoires non-volatiles à grille flottante", P. Normand, IMEP, MINATEC, Grenoble, France, 24 June 2008.

### Conference Organisation

1. 34th International Conference on Micro- and Nano-Engineering, MNE 2008, Athens, Greece, September 15-19, 2008. (www.mne08.org ). This conference was organized by the Institute of Microelectronics (IMEL) from NCSR Demokritos. Organizing Committee: E. Gogolides (Conference Chair), A. Tserepi (Conference Co-Chair), I. Raptis (Program Chair), P. Normand (Program Co-Chair), P. Argitis, N. Glezos, K. Misiakos, M. Hatzakis (Honorary Member).

### Patent

1. Greek Patent Application, No 20080100269, Publication date: 18-04-2008, Memory devices using proton-conducting polymeric materials, Inventors: E. Kapetanakis, A.M. Douvas, D. Velessiotis, E. Makarona, P. Argitis, N. Glezos, P. Normand.