PROJECT II.1

NANOSTRUCTURES FOR NANOELECTRONICS, PHOTONICS AND SENSORS

Project Leader: A. G. Nassiopoulou

Permanent Researcher: S. Gardelis

Post Doctoral Scientists: E. Hourdakis, V. Gianneta, A. Sotiropoulos

PhD Students: P. Manoussiadis, P. Sarafis, I. Leontis, K. Valalaki

OBJECTIVES

The activities of the group focus in the following:

a) Si nanowires and nanocrystals

Historically the activity on semiconductor nanostructures started within this research group at the early nineties and is conducted within different EU projects. Worldwide pioneering results of the group in this field include the following: The group was the first to report on the fabrication and light emitting properties of Si nanowires (APL 66(9), 1114 (1995)), and on an electroluminescent device based on vertical Si nanowires (APL 69(15), 2267 (1996)). The growth of single and multilayered two-dimensional arrays of Si nanocrystals (NCs) with controllable size embedded in SiO_2 was also reported in the nineties, Si NC memories with good characteristics using LPCVD Si nanocrystal were also developed.

In 2012 the group focused on the following:

- Synthesis, characterization and applications of SiNWs by metal-assisted chemical etching:
- Fabrication and properties of two-dimensional arrays of Si nanocrystals embedded in SiO_2 for solar cell applications

b) *Porous Si*

The group has important expertise and know-how in porous Si formation, properties and applications. Highly porous Si is a nanostructured material composed of interconnected nanowires and nanocrystals. Due to its structure and morphology, porous Si has interesting properties, including its very low thermal conductivity and its tunable dielectric permittivity. Based on the above properties, it finds important applications in thermal isolation and in RF shielding on the Si wafer. Pioneering results of the group over the years using porous Si include the development of efficient porous Si micro-hotplate technology on the Si wafer, a low power Si flow sensor, a flow meter for the car engine and a system for respiration control using the low power flow sensor. Developed processes include the local formation of porous Si thick films formed locally on the Si wafer, porous Si free standing close-type membranes over cavity fabricated in a single electrochemical process and porous Si cantilevers and suspended membranes fabricated by electrochemistry.

In 2012 the group focused on the development of porous Si as an RF substrate material and as a substrate material for cooling and heating devices. Its dielectric permittivity was investigated as a function of material porosity, structure and morphology for the frequency range 0-210 GHz. Its thermal properties were also investigated at both room and low temperatures down to 20K for cryogenic applications. Finally, the growth of metal nanoparticles and nanowires within the pores of the porous Si material is being studied.

c) Porous anodic alumina thin films on Si

The formation, properties and applications of porous anodic alumina thin films on Si are investigated. Highly ordered hexagonal pore arrangement is achieved by electrochemical oxidation of Al films on Si. The applications developed include the formation of nanowires within and the use of porous alumina films on Si as a masking material for Si nano-patterning. Porous anodic alumina has been also investigated as a high-k dielectric material in memory devices and in metal-oxide-metal (MIM) capacitors.

Key results in 2012

- ⇨ Porous Si thermal conductivity was determined in a wide temperature range of 20–350K. Porous Si shows a much lower thermal conductivity than bulk crystalline Si, this difference exceeding four orders of magnitude at temperatures below 50K.
- ⇨ The dielectric properties of porous Si for its use as a local RF substrate on the Si wafer were investigated in detail. Co-planar waveguides and inductors were fabricated on local porous Si areas on the Si wafer and tested at radiofrequencies.
- ⇨ A detailed comparison was made between porous Si as a local RF substrate and the state-of-the-art RF substrate trap-rich high resistivity (HR) Si. The comparison revealed the important advantages of porous Si for this application, compared to the trap-rich HR Si.
- ⇨ The kinetics of growth of Ni nanoparticles and nanowires into porous Si layers were investigated. The porous Si layers had vertical branched pores of average diameter in the range of 30-45nm. The porous Si layer thickness was in the range of 0.5 to 4 μm. The growth of the Ni nanoparticles and nanowires was achieved using pulsed electrodeposition from a Ni salt solution.
- ⇨ Si nanopatterning through an on-chip self-assembled porous anodic alumina (PAA) masking layer using reactive ion etching based on fluorine chemistry was investigated. The pattern of the hexagonally arranged pores of the alumina film was perfectly transferred to the Si surface.

Infrastructure Development

The electrochemistry laboratory was fully upgraded in 2012
The sputtering system in the laboratory was upgraded. The following materials are deposited: amorphous Si, SiO_2, Al, Cu and Pt.
The optics laboratory for PL, photocurrent and solar cell characterization was also upgraded.

FUNDING

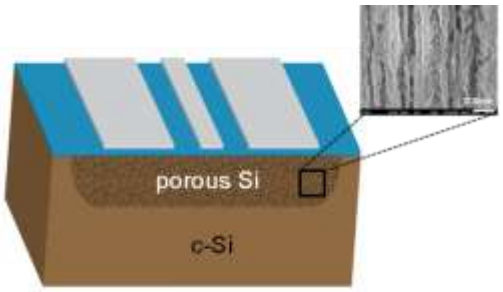
- EU FP7 ENIAC JU Project SE2A, 1/1/2009-31/03/2012- Contract No 120009
- EU FP7 Network of Excellence NANOFUNCTION, 1/9/2010-31/8/2013 - Contract No 257375
- EU FP7 Coordination and Support Action NANO-TEC, 1/9/2010-28/2/2013 - Contract No 257964

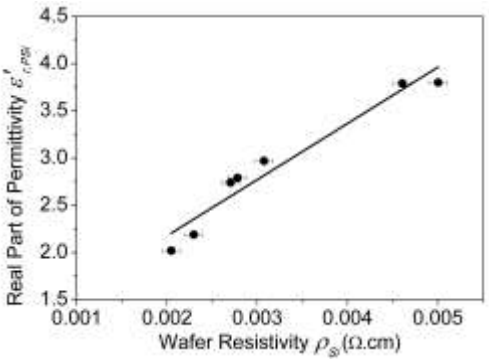
MAIN RESULTS in 2012

A. Porous Si as an RF substrate material. Investigation of its dielectric properties

P. Sarafis, M. Hourdakis and A. G. Nassiopoulou

The dielectric properties of porous Si for its use as a substrate material in Si-integrated RF passive devices were investigated and its advantages for this application were demonstrated. The greatest advantage is that porous Si can be combined with CMOS processing and local areas on the Si wafer can be formed, providing an efficient local RF shielding platform on the lossy Si substrate. High performance RF passive devices can be integrated on the local porous Si areas. Co-planar waveguide transmission lines were integrated on porous Si and their performance at RF was assessed [A1].





The dielectric permittivity of porous Si layers formed on a low resistivity p-type Si (0.001-0.005 Ω·cm) has been thoroughly investigated in the frequency range 1-40 GHz using analytical expressions within the framework of the broadband transmission line characterization method [A1]. It has been demonstrated that the value of Si resistivity is critical for the resulting porous Si layer permittivity even within the above limited resistivity range. Indeed, the real part of porous Si dielectric permittivity changes monotonically between 1.8 and 4 by changing the Si resistivity between 0.001 and 0.005 Ω·cm (see the graph on the right). The above study was made for porosities between 70 and 84%. The quality factor and attenuation loss of the investigated co-planar waveguide transmission lines were found to be equal to Q=26 and a=0.19dB/mm respectively at 40GHz. These values are competitive to those obtained on quartz, which is one of the off-chip RF substrates with the lowest losses.

[A1] P. Sarafis, E. Hourdakis, and A. G. Nassiopoulou, “Dielectric Permittivity of Porous Si for use as Substrate Material in Si-Integrated RF Devices,” IEEE Transactions on Electron Devices, vol. 60, no. 4, pp. 1436–1443, Apr. 2013 (accepted in 2012).

B. Comparison between Si-based RF substrates for passive devices

P. Sarafis[1], M. Hourdakis[1], A. G. Nassiopoulou[1], C. Roda Neuve[2], K. Ben Ali[2] and J.-P. Raskin[2]
1. NCSR Demokritos, Greece, 2. UCL Belgium

Two novel RF substrate technologies have been compared, namely local porous Si RF substrate technology and high resistivity Si with a trap-rich layer on top (trap-rich HR-Si) [fig. B1]. Using standard Si processing, identical co-planar waveguide transmission lines, crosstalk structures

and test inductors were fabricated on the above two substrates, as well as on quartz and on standard p-type Si (fig. B1).

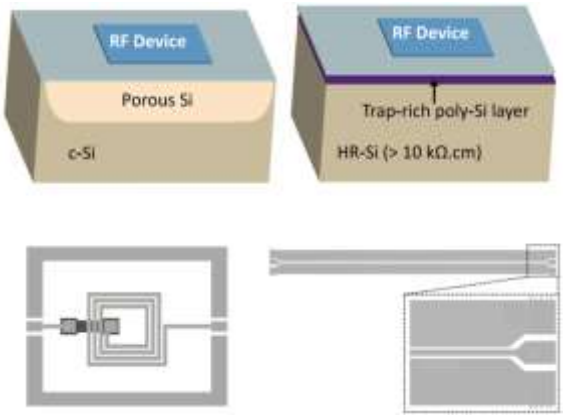


***Fig. B1**. Up-left: Cross-sectional illustration of the local porous Si areas on the Si wafer: Up right: HR-Si with the trap-rich layer on top. Down left: Layout of the square inductors. Down right: Layout of the CPW transmission lines integrated on the two above substrates under comparison.*

Broadband electrical characterization in the frequency range from 40 MHz to 40 GHz revealed that porous Si substrate provides much higher effective resistivity and lower dielectric constant than trap-rich HR-Si, that is comparable with values of a quartz substrate values (see Table I).

TABLE I.

Electrical Characteristics		Substrates: Quartz	Porous Si	Trap-rich HR-Si	p-type Si (1-10 Ω.cm)
CPW TLine characteristics	Zc (Ω)	78	100	51	34
	$\varepsilon_{r,eff}$	2.5	2.2	5.7	7.2
	α [@ 40 GHz] (dB/mm)	0.23	0.24	0.37	11.4
	Q [@ 40 GHz]	24.9	22.4	23.3	1.0
P_{out} in 2nd Harm. Distortion [@ P_{out} = 15 dBm] (dBm)		< -110	< -110	-90	> -40
Crosstalk [@ 25 GHz] (dB)		-22	-25	-15	-15

COMPARISON OF THE DIFFERENT SUBSTRATES

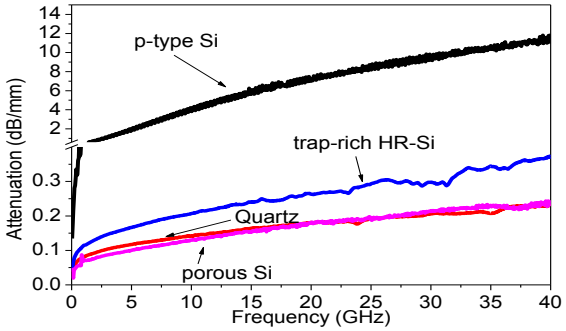


***Fig. B2.** Attenuation constant of the CPW transmission line as a function of frequency for the following devices on porous S, trap-rich HR-Si, quartz and p-type Si (1-10 Ω.cm). The CPW TLine on porous Si shows an attenuation constant as low as that on quartz.*

The higher effective substrate resistivity leads to lower attenuation losses (Fig. B2) and reduced non-linearities, as well as better quality factor for both transmission lines and inductors. In addition, the lower dielectric permittivity of porous Si leads to drastic reduction of crosstalk, to higher operating frequencies for inductors and provides design options for higher characteristic impedance devices.

Conclusively it can be said that porous Si, which is CMOS-compatible and cost-efficient, demonstrates state-of-the-art RF performances even comparable with the off-chip quartz substrate.

C. Thermal conductivity of porous Si at cryogenic temperatures

K. Valalaki and A. G. Nassiopoulou

Porous Si thermal conductivity was determined in a wide temperature range from 20–350K using the steady state dc method and a subsequent Finite Element Method (FEM). The method was applied to a 40 μm thick porous Si layer of ~60% porosity, formed on p-type Si (fig.C1). Our results on PSi were also compared with theoretical ones and were in good agreement with them. The main conclusions of this work are as follows: Porous Si shows much lower thermal conductivity than bulk crystalline Si, this difference exceeding four orders of magnitude at temperatures below 50K, as it is shown in fig.C2. The variation of porous Si thermal conductivity with temperature is monotonic and does not show any maximum for the measured temperature range, as in the case of bulk crystalline Si and other dielectric materials.

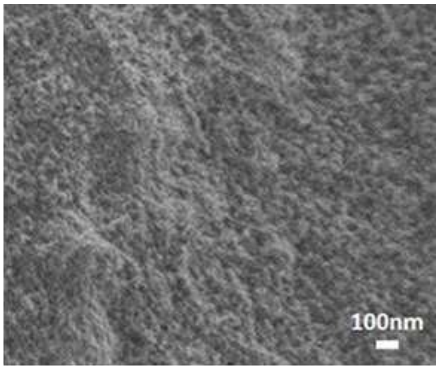


Fig. C1. *Cross sectional SEM image of the studied porous Si layer*

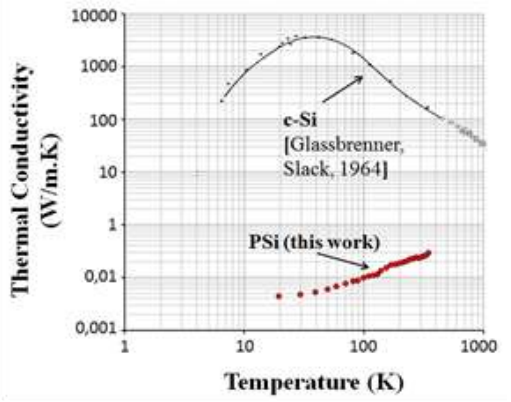


Fig. C2. *Comparison between thermal conductivity of porous Si (this work) and bulk crystalline Si (results from literature) as a function of temperature.*

Phonon confinement in Si nanostructures composing porous Si and phonon-wall scattering, are the basic mechanisms involved, and are at the origin of the above temperature dependence. The effectiveness of local thermal isolation from the Si substrate by a thick highly porous Si layer in a wide temperature range was demonstrated, showing that this material is challenging for use in Si micro-cooling devices.

Part of this work was presented in the 5th International Conference Micro & Nano 2012 on Micro - Nanoelectronics, Nanotechnologies and MEMS which held in Heraklion of Crete on 7-12 October 2012 as oral presentation.

Funding for this work was received from the European Union's 7th Framework Programme (FP7/2007-2013) through the ICT NoE project ‘Nanofunction’ (grant agreement number 257375).

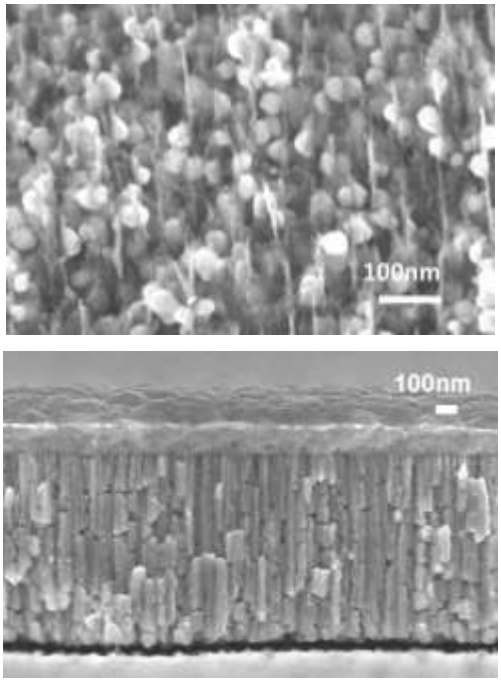
D. Mesoscopic Ni particles and nanowires into porous Si by pulsed electrodeposition

E. Michelakaki, K. Valalaki and A. G. Nassiopoulou

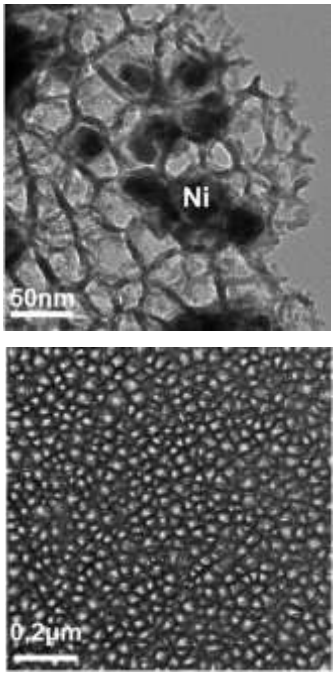
The kinetics of growth of Ni nanoparticles and nanowires into porous Si layers with vertical branched pores of average diameter in the range of 30-45nm and layer thickness in the range of 0.5 to 4 μm, using pulsed electrodeposition from a Ni salt solution were investigated. The effect of pulse duration, number of pulses and total process time on pore filling was investigated for porous Si with different porosities and porous Si layer thicknesses. SEM and TEM were used to characterize the samples. It was demonstrated that at the beginning of electrodeposition, nucleation of Ni nanoparticles on the pore walls takes place, following the Volmer-Weber growth mode. These nanoparticles are dispersed in the whole pore length. By increasing the number of pulses of a given duration, the size of Ni nanoparticles increases by diffusion-controlled growth

and neighboring nanoparticles coalesce into larger ones, until a continuous Ni nanowire is formed within the pores. By increasing the layer porosity, the obtained Ni nanoparticles were larger, resulting in all cases in a continuous Ni nanowire, fully filling the pore. By changing the porous Si layer thickness, the final result was qualitatively the same, but the intermediate result was different. Under similar total electrodeposition duration, in the thinner porous Si layer the size of Ni nanoparticles was larger than in the thicker one. However, by increasing the deposition time the pores were also fully filled with Ni in the case of the thicker porous Si layers. From the beginning of the process a metal film starts to form on the porous Si surface and its thickness increases with process time. However, the presence of this film does not impede further pore filling and nanowire formation into the pores. This supports further the diffusion controlled growth mechanism. Finally, it was demonstrated that full pore filling and continuous Ni nanowire formation is also achieved under direct current electrodeposition and the results are quite similar with those obtained with pulsed electrodeposition when the same total deposition time is used in both cases.

The research leading to these results has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement NANOFUNCTION n°257375.



Cross section SEM images of Ni-filled porous Si layers



TEM images from a surface area of Ni filled porous Si sample

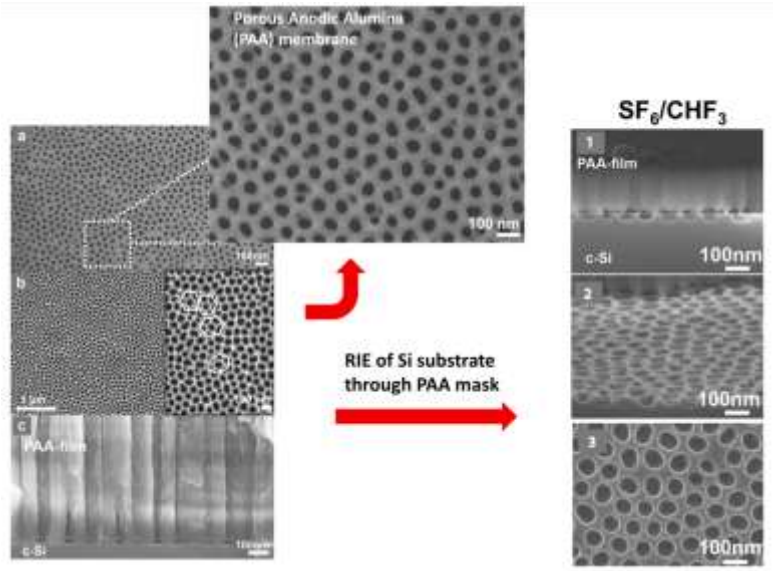
[D1]: E. Michelakaki, K. Valalaki and A. G. Nassiopoulou, “Mesoscopic Ni particles and nanowires by pulsed electrodeposition into porous Si”, Journal of Nanoparticle Research, Volume 15, Issue 4, 2013 (accepted 2012)

E. Si nanopatterning through porous anodic alumina mask

G. Violetta, A. Olziersky and A. G. Nassiopoulou

Si nanopatterning through an on-chip self-assembled porous anodic alumina (PAA) masking layer using reactive ion etching based on fluorine chemistry was investigated. Three different gases/gas mixtures were investigated: pure SF_6, SF_6/O_2, and SF_6/CHF_3. For the first time, a systematic investigation of the etch rate and process anisotropy was performed. It was found that

in all cases, the etch rate through the PAA mask was 2 to 3 times lower than that on non-masked areas. With SF_6, the etching process is, as expected, isotropic. By the addition of O_2, the etch rate does not significantly change, while anisotropy is slightly improved. The lowest etch rate and the best anisotropy were obtained with the SF_6/CHF_3 gas mixture. The pattern of the hexagonally arranged pores of the alumina film is, in this case, perfectly transferred to the Si surface. This is possible both on large areas and on restricted pre-defined areas on the Si wafer.



[E1] V. Gianneta, A. Olziersky and A. G. Nassiopoulou, "Si nanopatterning by reactive ion etching through an on-chip self-assembled porous anodic alumina mask", Nanoscale Research Letters, Volume 8, Issue 71, 2013 (accepted 2012)

F. Photo-electrical investigation of Si nanocrystals for photovoltaic cells

P. Manousiadis, S. Gardelis, and A.G. Nassiopoulou

Motivated by the potential use of Si nanocrystals (SiNCs) as absorber material in Si-based photovoltaic designs, we have grown single and multilayered nanocrystalline Si (nc-Si) films containing SiNCs of controlled sizes on quartz by low pressure chemical vapour deposition (LPCVD) of Si and subsequent oxidation at high temperature. The thickness of the nc-Si layers ranged from less than 2 nm up to 25 nm, by choosing suitable growth conditions. The multilayered films consisted of five nc-Si/SiO_2 bilayers. The structure of the films was investigated by high resolution transmission electron microscopy (HRTEM). From optical transmission and reflection measurements, energy band gaps of the SiNCs within the films were estimated and the results were correlated with the sizes of the SiNCs, as observed by HRTEM. Also the light emission properties of the films were investigated by photoluminescence measurements. Finally, photocurrent was measured. Electron microscopy showed that the films had columnar structure, i.e., they consisted of SiNCs with the z-dimension equal to the film thickness and with lateral sizes with narrow size distribution (Fig. F1(a)).

(a) **(b)**

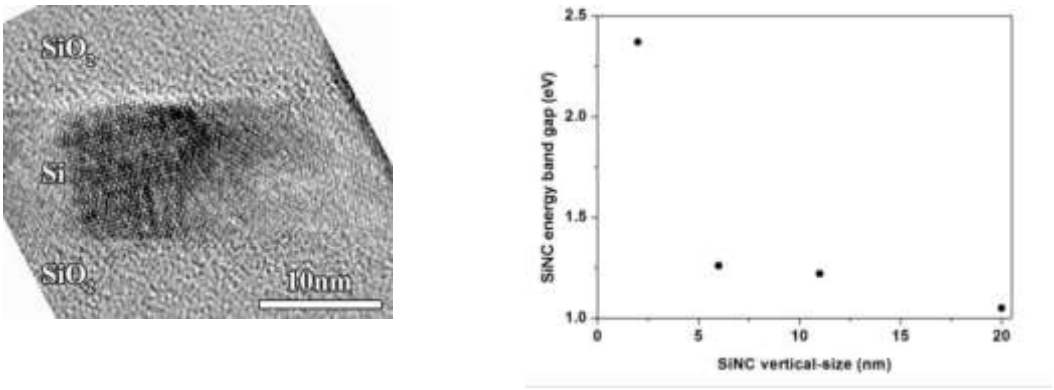


Fig. F1. *(a) Cross-section HRTEM image showing a SiNC. (b) Estimated energy band gap of the SiNCs within the different films*

The majority of the films had SiNCs touching each other without any observable oxidation at the grain boundaries. Only in the case of the thinnest film (SiNC vertical dimension ~ 2 nm) the SiNCs were well separated by silicon dioxide barriers. Absorption and energy band gaps of the SiNCs within the different films were deduced from suitable analysis of the optical transmission and reflection measurements. A shift of the energy band gap with decreasing SiNC was observed, which was consistent with quantum size effects in the SiNCs (Fig. F1(b)). The film containing the smallest SiNCs (with vertical dimension ~ 2 nm), besides a significant shift of the absorption edge to higher energies, showed light emission at room temperature which was due to the radiative recombination of photo-generated excitons in the localized SiNCs separated by SiO_2 tunnel barriers (Fig. F2(a)). Spectral dependence of the photocurrent coincided with the spectral dependence of the absorption (Fig. F2(b)). Specifically, photocurrent showed similar shift to higher energies as the size of the SiNCs decreased, confirming quantum size effects in the constituent SiNCs.

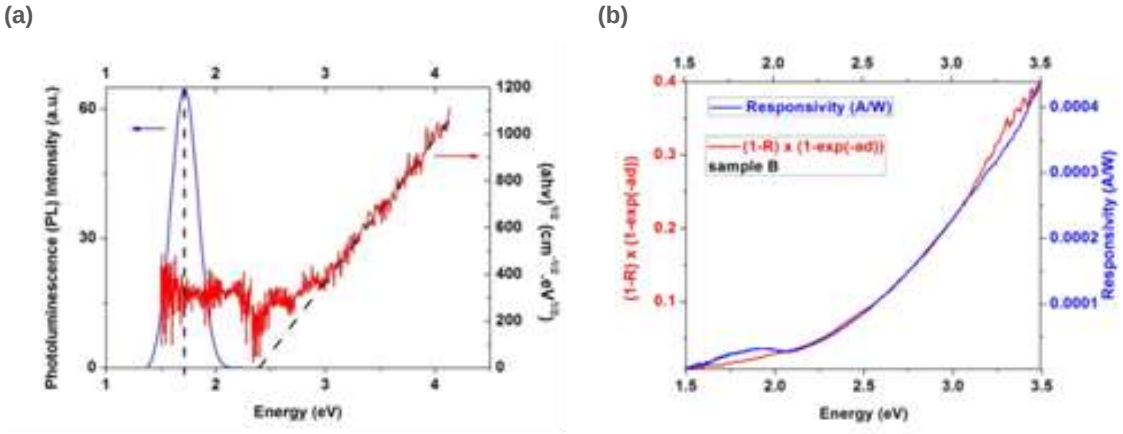


Fig. F2. *(a) Photoluminescence and absorption edge of 2nm SiNCs embedded in SiO_2. (b) Spectral dependence of responsivity (photocurrent normalized to the power of incident light) compared with the spectral dependence of the absorbed light.*

[F1] S. Gardelis, A.G. Nassiopoulou, P. Manousiadis, S. Milita, A. Gkanatsiou, N, Frangis, and Ch. B. Lioutas, "Structural and optical characterization of two-dimensional arrays of Si nanocrystals embedded in SiO_2 for photovoltaic applications", J. Appl. Phys. 111 (8), 0835346 (2012)

[F2] P. Manousiadis, S. Gardelis, and A.G. Nassiopoulou, "Lateral electrical transport and photocurrent in single and multilayers of two-dimensional arrays of Si nanocrystals", J. Appl. Phys. 112 (4), 043704 (2012)

PROJECT OUTPUT in 2012

Publications in International Refereed Journals

1. *High performance MIM capacitor using anodic alumina dielectric,*
   Hourdakis, E. and Nassiopoulou, A.G.
   Microelectronic Engineering, vol. 90, pp. 12-14 (2012)
2. *Novel Air Flow Meter for an Automobile Engine Using a Si Sensor with Porous Si Thermal Isolation,*
   E. Hourdakis, P. Sarafis and A. G. Nassiopoulou
   Sensors vol. 12 (11), pp. 14838-14850 (2012)
3. *Two-Terminal Charge-Trapping WORM Memory Device Using Anodic Aluminum Oxide"*
   Hourdakis, E. and Nassiopoulou, A.G.
   J. Nanosci. Nanotechnol. vol. 12 (10), pp. 7968-7974 (2012)
4. *Structural and optical characterization of two-dimensional arrays of Si nanocrystals embedded in SiO_2 for photovoltaic applications,*
   S. Gardelis, A. G. Nassiopoulou, P. Manousiadis, S. Milita, A. Gkanatsiou, N. Frangis, Ch. B. Lioutas, Journal of Applied Physics 111 (8), 083536 (2012)
5. *Lateral electrical transport and photocurrent in single and multilayers of two- dimensional arrays of Si nanocrystals,*
   P. Manousiadis, S. Gardelis, and A. G. Nassiopoulou
   Journal of Applied Physics 112 (4), 043704 (2012)

Published Conference Proceedings

1. *Arsenic Redistribution After Solid Phase Epitaxial Regrowth Of Shallow Pre-Amorphized Silicon Layers,*
   E. Demenev, D. Giubertoni, S. Gennaro, M. Bersani, E. Hourdakis, A. G. Nassiopoulou, M. A. Reading and J. A. van den Berg
   AIP Conf. Proc. 1496, 272 (2012)

Conference Presentations – Invited Talks

1. *Two terminal WORM device based on charge-trapping in porous anodic alumina,*
   E. Hourdakis and A.G. Nassiopoulou
   Micro&Nano 2012, Heraklion, Crete, Greece
2. *Arsenic redistribution after solid phase epitaxial regrowth of ultra-thin pre-amorphized silicon layers,*
   E. Demenev, D. Giubertoni, S. Gennaro, M. Bersani, E. Hourdakis, A. G. Nassiopoulou, M. A. Reading, and J. A. van den Berg
   International conference on Implantation Technology 2012, Valladolid, Spain
3. *Two-terminal charge-trapping WORM memory device using porous anodic alumina,*
   E. Hourdakis and A. G. Nassiopoulou
   E-MRS 2012, Strasbourg, France (poster)
4. *Role of surface chemical treatment on the optical properties of SiNWs fabricated by single step metal assisted chemical etching,*
   I. Leontis, A. G. Nassiopoulou and A. Othonos
   XXVIII Panhellenic Conference on Solid State Physics and Materials Science 2012, Patra, Greece
5. *Room and low-temperature thermal conductivity measurements of highly porous Si with nanostructured morphology,*
   K. Valalaki and A. G. Nassiopoulou
   Micro&Nano 2012, Heraklion, Crete, Greece
6. *Porous Si substrate technology for RF passives integration,*
   A. G. Nassiopoulou
   Workshop on Nanoelectronic Materials and Devices, organized by Micro&Nano, Athens, 17 December 2012 (invited)
7. *High performance RF passive devices in CMOS technology on a local porous Si substrate,*
   A. G. Nassiopoulou
   Workshop on Recent Developments in Nanoelectronics, Thessaloniki, 3 June, 2012 (invited)
8. *Nanostructured Si in the "More than Moore" Nanoelectronics field,*
   A. G. Nassiopoulou

XI International Conference on Nanostructured Materials, 26-31 August 2012, Rhodes Greece (invited)

9. *Nanostructured porous Si as a local on-chip RF microplate for high performance RF device integration,*
   A. G. Nassiopoulou
   Workshop on Novel Materials, Devices and technologies for High performance RF applications, organized within the ESSDERC/ESCIRC Conference, Bordeaux France, 21 September 2012
10. *ECOSYSTEMS TECHNOLOGY & DESIGN for NANOELECTRONICS: a European Coordination Action: NANOTEC,*
    A. G. Nassiopoulou
    Tutorial, organized within the ESSDERC/ESCIRC Conference, Bordeaux France, 21 September 2012
11. *Optical properties, electrical transport and photocurrent in single and multilayered Silicon nanocrystal films,*
    S. Gardelis, P. Manousiadis, and A.G. Nassiopoulou
    EMRS 2012, Spring Meeting, Strasbourg, France
12. *Single and multilayers of two-dimensional arrays of Si nanocrystals for photovoltaics: Structural and optical characterization,*
    S. Gardelis, A. G. Nassiopoulou, P. Manousiadis, A. Gkanatsiou, N. Frangis, Ch. B. Lioutas
    XXVIII Panhellenic Conference on Solid State Physics and Materials Science 2012, Patra, Greece
13. *Electrical transport and photocurrent in two-dimensional arrays of silicon nanocrystals for photovoltaic applications,*
    S. Gardelis, P. Manousiadis, and A. G. Nassiopoulou
    Micro & Nano 2012, Heraklion, Grete, Greece

Teaching and Training Activities

1. Lectures on “Silicon processing for Nanoelectronics” by A. G. Nassiopoulou and E. Hourdakis within:
   a) the MSc program on Microelectronics organized by the Department of Informatics of the University of Athens, in cooperation with the Department of Microelectronics of NCSR Demokritos and
   b) the MSc program on “Microsystems and Nanoelectronics” organized by the National Technical University of Athens with the participation of the Department of Microelectronics of NCSR Demokritos
2. Lectures on “Micromechanics and Sensors”, by the S. Gardelis within the MSc program organized by the: Department of Informatics, University of Athens, in cooperation with the Department of Microelectronics of NCSR Demokritos