

Specific Electrical Measurement Techniques for the Study of Silicon NanoStructures.

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Adding functionalities to microelectronics chips can be done by the integration of more devices, such as MIM capacitors. However new functionalities arising from new devices and concepts are probably the most promising. With the size reduction of the different features of microelectronic devices, we observe a clear evolution towards nanoelectronics, where new phenomena appear. While leading to physical limitations in classical MOS devices, phenomena such as tunneling and Coulomb blockade can be exploited to realize new devices. First we will focus on 'nano-inside' devices: non-volatile memories, where silicon nanocrystals (Si-nc) play a key role and are one of the most promising device exploiting mono-electronic properties. Then we will consider 'full nano' devices where nanostructures are designed by AFM lithography. We will show how the material and electronic transport properties of these nanostructures can be explored from several original electrical measurements, such as quasistatic capacitance measurements, constant capacitance method, low frequency noise analysis, etc. Finally, we will present nano electro mechanical systems (NEMS) that are currently under study.

Laurent Montès received his Ph.D. in microelectronics from the Université Joseph Fourier de Grenoble in 1999. In 2000, he was a postdoctoral fellow at the University of Rochester, NY-USA. In 2001 he became an Assistant Professor at INP-Grenoble, where he became an Associate Professor in 2002. His research interests include microelectronics, nanotechnologies, nanosilicon memories, nanowire devices and micro-nano-systems (MEMS/NEMS) with strong industrial and international partnerships. His teaching activities include lectures in nanoelectronics, nanostructures for optics and measurement techniques. He is director of MIGAS, an international summer school on advanced microelectronics. He was also involved in the set-up of the European School On Nanosciences and Nanotechnologies (ESONN) and the International Master in Micro and Nano Technologies for Integrated Circuits (Nanotech) between INP-Grenoble in France, Politecnico di Torino in Italy and EPF-Lausanne in Switzerland.