Langmuir–Blodgett Film Deposition of Metallic Nanoparticles and Their Application to Electronic Memory Structures

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ABSTRACT

The Langmuir–Blodgett deposition of organically passivated gold nanoparticles is reported. A monolayer of these particles has been incorporated into a metal–insulator–semiconductor (MIS) structure. The MIS device exhibits a hysteresis in its capacitance versus voltage characteristic, the magnitude of which is dependent on the voltage sweep conditions. Charge storage in the layer of nanoparticles is thought to be responsible for this effect.

Nanoparticulate materials of semiconductors1-2 and metals3-4 are currently the focus of intense research. The physical properties of such small-scale structures can be tailored for particular applications. For example, their electronic and chemical behavior can be changed simply by controlling the particle size. Nanoparticles also provide useful building blocks from which complex molecular architectures may be built. In the field of microelectronics, the 1–20 nm size typically associated with nanoparticles allows high device densities to be achieved. Quantum mechanical effects, such as Coulomb blockade, may also be exploited in device structures such as the single-electron transistor.5

Over the past few decades, the evolution of microelectronic devices based on complementary metal oxide semiconductor (CMOS) technology has followed Moore’s law, namely that the number of functions per chip double every 1.5 years. The semiconductor industries anticipate a significant increase in the density of the transistors in both the microprocessor unit (MPU) and the dynamic random access memory (DRAM) of a CMOS chip over the next decade.6 The prediction is for a 30 nm minimum feature size (gate length) for the MPU and 1010 transistors per cm2 in the case of the memory by the year 2012. These figures are regularly updated.

An important MOS device is flash memory.7 This is similar in structure to a MOS field effect transistor (MOSFET), except that it has two gate electrodes, one on top of the other. The top electrode forms the control gate, below which a “floating” gate is capacitively coupled to the control gate and the underlying silicon. The memory cell operation involves putting charge on the floating gate or removing it, corresponding to two logic levels. Nanoflash devices utilize single or multiple nanoparticles as the charge storage elements. These are usually embedded in the gate oxide of a field effect transistor and located in close proximity (2–3 nm) to the transistor channel.8 Floating gates consisting of Si or Ge nanocrystals have been fabricated through the use of various techniques or ion beam synthesis.9-11

The Langmuir–Blodgett (LB) technique is a room-temperature deposition process that may be used to deposit monolayer and multilayer films of organic materials. Furthermore, this method permits the manipulation of organic molecules on the nanometer scale, thereby allowing intriguing superlattice architectures to be assembled.12 Here, we report on the LB deposition of gold nanoparticles and on preliminary investigations of their incorporation into a simple
capacitor structure. It is hoped that the experiments will provide some insight into the feasibility of fabricating high density, low-cost charge-storage elements based on organic thin films.

The gold nanoparticles (Q-Au) were of nominal diameter 10 nm passivated with tri-n-octylphosphine oxide/octadecylamine; a schematic diagram of their structure is shown in Figure 1. This capping makes the nanoparticles soluble in various organic liquids, but mainly insoluble in water; the Q-Au is thus suitable for LB deposition. The organically passivated nanoparticles were prepared as previously described using Schlenk line techniques. In a typical preparation, 10 g octadecylamine, 25 g technical grade tri-n-octylphosphine oxide (TOPO) and 0.0325 g NaBH₄ were charged to a Schlenk flask, the atmosphere evacuated and back flushed with dry nitrogen three times. The organic ligands and reducing agent were then heated under vacuum to 100 °C for an hour, and finally flushed with dry nitrogen. The temperature was increased and stabilized at 190 °C. A solution of HAuCl₄ (0.07 g, 2.0 × 10⁻⁴ M) in 5 mL of 4-tertiary butylpyridine was injected directly into the hot organic ligands, causing an immediate deep red coloration. The solution was allowed to grow for 30 min under dry nitrogen, and then removed from the heating source. The solution was allowed to cool to 60 °C, removed from the Schlenk line, and ca. 50 mL of methanol added, causing a precipitate. This was isolated by centrifugation, giving a dark red powder, which could be dispersed in nonpolar organic solvents, such as toluene. Filtration of the toluene solution yielded a dark red solution of gold nanoparticles with a cubic crystalline core, capped with a mixture of TOPO and octadecylamine.

Langmuir–Blodgett film deposition was undertaken using a Molecular Photonics LB700 trough situated in a class 10,000 microelectronics clean room. The subphase was purified water obtained from a reverse osmosis/deionization/UV sterilization system; the film depositions were undertaken at a subphase pH of 5.8 ± 0.2 and a temperature of 20 ± 2 °C. Cadmium arachidate (CdAA) films were obtained by spreading arachidic acid (Sigma Aldrich, purity 99%) on a water subphase containing 5.0 × 10⁻⁴ M cadmium chloride (BDH, Aristar Grade). The deposition pressure for these fatty acid salt films was 22 mN m⁻¹. Transmission electron microscopy (TEM) studies were undertaken using a JEOL 200CX microscope.

Silicon (p-type, (100) orientation, resistivity 1–2 Ω cm) wafers with a 3.8 nm thermally grown oxide layer were used as the substrates. Ohmic back contacts were first formed by the thermal evaporation of Al (thickness 300 nm) and subsequent annealing at 490 °C for 10 min in a nitrogen ambient. Following LB deposition, Al top contacts (thickness 300 nm, 1 mm diameter) were thermally evaporated in a vacuum chamber (pressure 10⁻⁶ mbar) onto the organic films through a metal shadow mask. Figure 2 shows the various metal/insulator/semiconductor (MIS) structures that were investigated in this work: (a) Al/SiO₂/p-Si; (b) Al/20 LB layers CdAA/SiO₂/p-Si; and (c) Al/20 LB layers CdAA/one LB layer Q-Au/SiO₂/p-Si.

The current voltage and capacitance–voltage characteristics of the MIS structures were measured using a PC-driven picoammeter (HP4140B) and an LCR bridge (HP4192).

Solutions of the nanoparticles were made using both chloroform (Merck, Aristar grade) and toluene (Sigma Aldrich, HPLC grade) at a concentration of nominally 0.5 g L⁻¹. Both gave similar results, but the rapid evaporation of the chloroform made it a more frequent choice. Figure 3 shows a surface pressure versus area isotherm taken using

Figure 1. Structure of Q-Au nanoparticle.

Figure 2. Schematic diagrams of different metal–insulator–semiconductor structures.
20 μL of Q-Au in CHCl₃ solution; the compression speed was 1 mm s⁻¹ (maximum surface area = 150 cm², LB trough compression ratio 5:1). The data are plotted in the form of surface pressure versus area occupied by the floating film on the subphase surface. Unfortunately, lack of detailed information about the nanoparticles (molecular weight, density) prevented the isotherm from being presented in the normal way (i.e., surface pressure versus area per molecule). Subsequent expansion and recompression of the floating film produced an isotherm close to that shown in Figure 3.

For transmission electron microscopy studies, a 3 mm TEM grid coated with a carbon film was mounted vertically using crossover tweezers. Following compression to 45 mN m⁻¹, LB deposition was attempted. No film transfer was noted during the downward movement of the substrate through the water/Q-Au interface; however LB film deposition with a low transfer ratio, ≈ 0.1, was noted on the upstroke. A resulting TEM micrograph is shown in Figure 4. The nanoparticles possess a well-ordered, close-packed arrangement, and what appear to be twins are evident by close inspection of some of the Q-Au particles. The average particle diameter is approximately 8 nm, although, as the TEM did not possess an accurate calibration, this value should be taken as having an error of up to 50%. Within the regions in which particles were present, the coverage was extremely dense. However, these areas only extended over distances of hundreds of nanometers, with the majority of the film being almost devoid of nanoparticles. This is most likely due to poor adhesion, and is, to some extent, in agreement with the low transfer ratio noted above.

Much improved LB deposition was found for transfer onto silicon substrates; in this case a lower deposition surface pressure, 22 mN m⁻¹ was found to be optimal. Prior to film transfer, the silicon substrate was treated with dimethyldichlorosilane to make the surface hydrophobic. Film deposition was evident on the first downward movement of the substrate, with a transfer ratio of 1.0 ± 0.05. However, no film transfer occurred on the first upstroke of the substrate. The deposition of subsequent layers was X-type, i.e., film deposition only on the downstroke. Up to 10 layers of Q-Au could be assembled onto gold; however, a small proportion, ≈ 10%, of the material seemed to come off the substrate during the upstroke as the multilayer film was built up.

Figure 5 shows the normalized capacitance versus voltage (C−V) data, measured at 1 MHz and a voltage sweep rate of 40 mV s⁻¹ for the three different device structures investigated. In each case, the voltage scan was started in the inversion region and swept toward accumulation. The C−V curve for the reference Al/SiO₂/Si sample (i.e., Figure 2a) reveals the usual accumulation/depletion/inversion characteristics associated with MIS structures, with a flat-band voltage of approximately −1 V. Negligible hysteresis was evident on reversing the voltage scan. The data for the Si/SiO₂/CdAA structure also show clear accumulation, depletion, and inversion regions, with no hysteresis on reversing the direction of the voltage scan and independent of the value of the voltage at which the scan commenced. The absolute value of the accumulation capacitance (≈ 255 pF) was consistent with that expected from the fatty acid film (20 layers) on top of the 3.8 nm SiO₂ layer.

The data in Figure 5 reveal that the flat band voltages of both LB film MIS devices are approximately −3 V, shifted by about 2 V when compared to the Si/SiO₂ device. This suggests that the fatty acid salt LB structure has some incorporated positive charge at the LB film/SiO₂ interface or within the insulator, i.e., a more negative potential has to be applied to the gate electrode to achieve the same flat band
conditions in the semiconductor. Such effects have been reported previously in MIS devices incorporating fatty acid and fatty acid salt insulators.\textsuperscript{14}

The most significant difference in the structures with and without the Q-Au nanoparticles is the relatively large hysteresis in the MIS structure containing the Q-Au layer. The clockwise nature of this hysteresis (for a p-type semiconductor) is usually associated with ion drift or polarization of the insulator.\textsuperscript{15} However, the lack of any hysteresis for the LB reference MIS sample (i.e., structure shown in Figure 2b) indicates that an alternative explanation may be more appropriate. We therefore suggest that charge storage in the Q-Au layer might account for the observed hysteresis. In accumulation (negative bias applied to the top metal electrode), electrons may be injected from the top electrode to the nanoparticles, which then become negatively charged. The opposite effect occurs in the inversion region, i.e., electrons are extracted from the nanoparticles to the top electrode. Previous work with LB film MIS devices based on GaP has shown that a relatively thick fatty acid film can support significant electron and hole currents, but the precise conduction mechanisms were unclear.\textsuperscript{16} Although the SiO\textsubscript{2} layer used in this work is relatively thin (3.8 nm), the distance between the surface of the silicon and the gold particles is effectively increased to over 5 nm because of the presence of the organic capping layer associated with the Q-Au. This may prevent easy charge transfer via tunneling from the semiconductor to the Au.

The charge storage effects were examined further by monitoring the C–V curves for different voltage sweeps, using an applied voltage step of 0.2 V and a step delay time of 1 s, Figure 6. Here, the scan starts from different voltages in the inversion region; the solid line corresponds to a sweep of ±4 V, the dashed line to ±5 V, and the dotted line to ±6 V. The magnitude of the hysteresis is expressed as a voltage shift that is proportional to the magnitude of the trapped charges in the insulator layer. This shift between the forward and reverse scans $\Delta V$ is estimated by

$$\Delta V = |V^- - V^+|$$

where $V^-$ and $V^+$ are the voltages of the forward and backward C–V curves measured at a capacitance value of 50 pF. The dependence of the hysteresis on the voltage limits of the C–V measurement is presented in the inset figure. To a first approximation, $\Delta V$ is proportional to the bias voltage limit.

In conclusion, Langmuir–Blodgett layers of organically capped gold nanoparticles have been successfully built up (X-type deposition) onto silicon/silicon oxide surfaces. Layers of cadmium arachidate were deposited on top of a single layer of the nanoparticles to form a metal–insulator–semiconductor structure. The capacitance versus voltage characteristics of these devices were shown to exhibit hysteresis when the voltage scan was reversed. This effect was dependent on the starting sweep voltage and attributed to the storage of charge in the nanoparticles. We are currently undertaking further work to establish the precise mechanism of charge storage (e.g., by using thinner SiO\textsubscript{2} and/or thicker LB insulator layers) and to attempt to incorporate the Q-Au layer into a FET structure.

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**Note Added After ASAP.** This paper was originally posted on the Web on 3/5/2003. Units of reference were added to the scale bar in Figure 4. The revised paper was reposted on the Web on 3/17/2003.

**References**

(6) Semiconductor Industry Association roadmap map, see website at: http://public.itrs.net/.