Project III. 1

POROUS SILICON TECHNOLOGY and APPLICATIONS

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Funding:

- EU Marie Curie/ ''RF on porous'', re-integration grant, Contract N^0 016142, 29/7/2005-28/7/2007
- Contract with the National Research Agency-Cyprus, Photothermal analysis, 1/7/2004-30/6/2006
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- Contract with the company ST Microelectronics SA France, RF-on-porous, 30/7/2005-30/7/2008

Research orientation:

- Porous silicon material development: mesoporous and macroporous silicon
- Development of silicon micromachining technologies using porous silicon
- Application in flow sensors, accelerometers, microfluidic devices and on-chip integration of RF components.

a) Porous silicon technology for sensors

A big effort has been devoted the last years at IMEL in developing materials and enabling technologies for application in sensors. One such material platform with important potential for applications in different sensor devices, microfluidics, lab-on-chip, integration of passives on silicon etc. is porous silicon technology.

Either nanostructured mesoporous or macroporous silicon are grown at IMEL. Mesoporous silicon is very appropriate for use as micro-plate for local thermal or electrical (dc, RF) isolation on a silicon substrate. Macroporous silicon is developed for use in photonics, via technology, device cooling and particle filtering.

Different technologies based on porous silicon are available at IMEL, including:

- Proprietary micromachining techniques based on the use of porous silicon as a sacrificial layer for the fabrication of free standing membranes, bridges and cantilevers on a silicon substrate
- Technologies using porous silicon for local thermal or RF isolation on a silicon wafer, or using porous silicon as a matrix for the deposition of catalytic materials for use in chemical sensors

b) RF isolation by porous silicon micro-plates on a silicon substrate

This activity is more recent at IMEL. The overall objective is:

- to explore and extend porous silicon technology into the domain of CMOS-compatible integrated RF systems for use in systems-on-chip and
- to improve the performance of currently integrated analog CMOS components by above technology transfer and related optimization of design methodologies.

RESEARCH RESULTS

A. Integrated inductors on Porous Silicon in CMOS-compatible processes

H. Contopanagos, D. Pagonis and A. G. Nassiopoulou

Radio-frequency (RF) components such as inductors, capacitors, filters, transformers and other resonators, integrated on-chip, are essential building blocks of all analog radio frequency integrated circuits (RFICs) and their performance at current and future CMOS processes is a major bottleneck to successful system integration, especially for single-chip radios at high frequencies. It is clear that fully on-chip inductors in a CMOS-compatible process substantially improving the current art would create an important competitive advantage in the overall performance/cost ratio compared to hybrid technologies. In this work we explored the use of porous silicon as a compact micro-plate with low RF losses, grown locally on the silicon substrate by electrochemistry, as a way to implement significantly higher-Q RF inductors on a standard CMOS technology. We have shown that using a 50μm-thick porous Si RF micro-plate on standard CMOS technology, respecting corresponding metallization foundry rules, increases the Q-factors of the inductors as follows: On 0.18μm CMOS (Al metallization), the Q-factor enhancement is 50%-60%. On 0.13μm CMOS and smaller-scale nodes (Cu metallization) the enhancement is about 100%. Using an in-home CMOS-compatible process allowing 2 metal layers, the corresponding maximum Q-factors for the same optimized metallization is 17 and 34 respectively. When a standard CMOS metal stack of 6 Cu layers is used, the maximum Q-factor reaches 50, which is comparable with the performance of much larger off-chip inductors. Of equal importance, the frequency shape of the Q-factors with porous Si benefits the higher wireless communications bands (Bluetooth-WLAN). Currently, we are working on RF electrical characterization of porous Si and we fabricate the corresponding inductors.

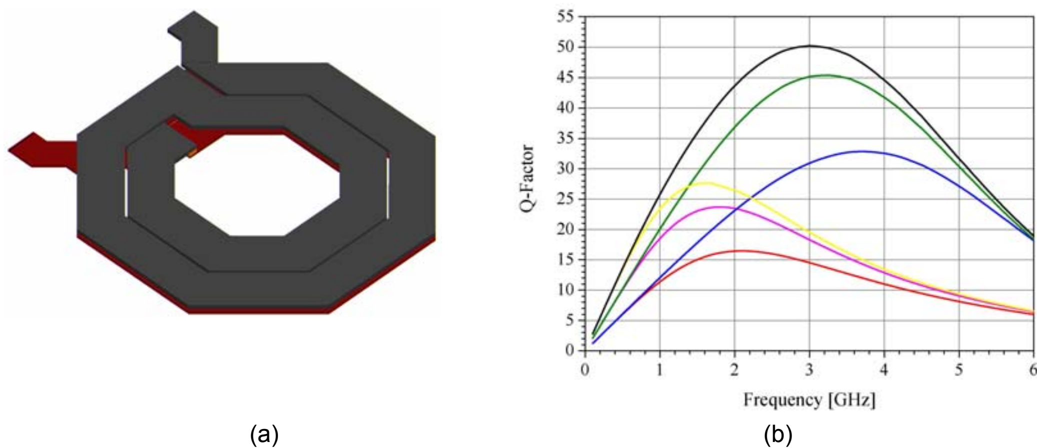


Fig. III.1.1: *a) Optimized 2-metal inductor layout: Grey = M2 (top metal); Brown = M1 (bottom metal closest to Si). b) Q-factors of optimized inductors of the same inductance and self-resonant frequencies for 0.13μm CMOS: Blue/Red = 2 metals with/without porous Si; Green/Magenda = 4 metals with/without porous Si; Black/Yellow = 6 metals with/without porous Si.*

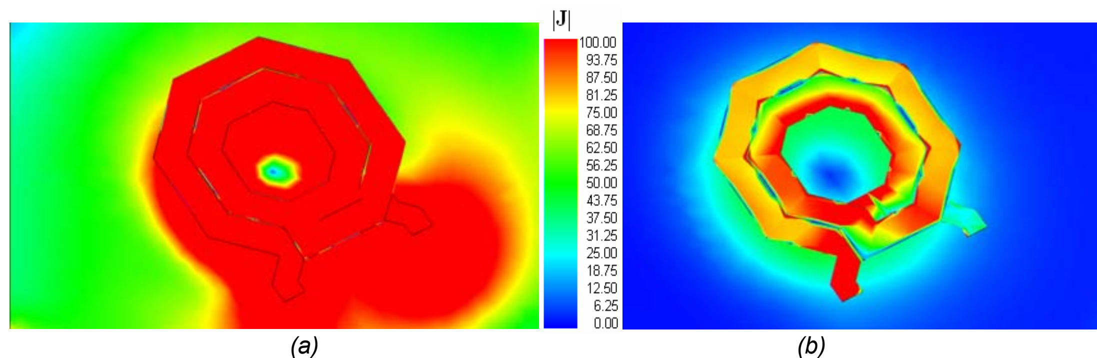


Fig. III.1.2: *Lateral current density magnitude distribution 50μm underneath M1: a) Without porous Si and b) with porous Si.*

B. Confined macroporous silicon membranes on pre-defined areas on the Si substrate

D. N. Pagonis and A. G. Nassiopoulou

In this work we investigated the formation of confined macroporous silicon membranes on pre-defined areas on the silicon substrate. Two different cases were considered: a) membranes supported by the silicon substrate and b) membranes suspended over a cavity on Si. The confined areas were defined lithographically and porous silicon formation took place at mask openings. The main difficulty to overcome was to avoid trenching and silicon over-etching at mask borders. A detailed study was undertaken to find an optimum masking material in order to avoid the trench formation at the borders of the lithographically defined areas. An appropriate masking technology was developed and used to fabricate a) single macroporous and b) bilayers of macroporous over mesoporous silicon. In the second case, by selectively removing the mesoporous layer, suspended confined macroporous silicon membranes over a cavity on the silicon substrate were fabricated (figure III.1.3).

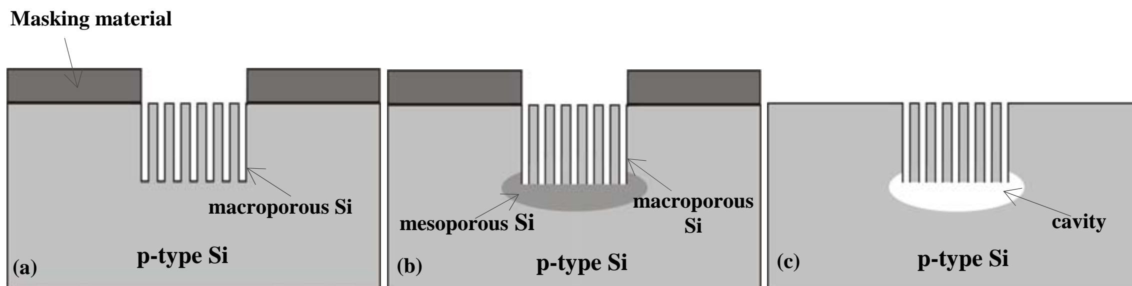


Fig.III.1.3: *Scematic representation for the formation process of free-standing macroporous membranes over a cavity; a) Formation of a confined macroporous silicon membrane through a lithographic mask; b) Formation of mesoporous Si underneath the macroporous layer; c) Mesoporous Si dissolution and cavity formation - Mask dissolution*

The new masking technique is based on the creation of n-type silicon areas by ion implantation. Appropriate experiments were carried out using the developed technology. Typical obtained results are presented in figures III.1.4a & III.1.4b below. Macroporous silicon membranes have been successfully formed locally only at the defined geometry by the n-type areas. There are no trenches created at the sides of the macroporous silicon membrane and there is no surface etching at the borders of the n-type area. The developed process is fully compatible with silicon processing for IC fabrication. The obtained results are promising and show an important potential for the fabrication of useful structures for different applications, as for example lab-on-chip and drug delivery systems. Although the technique needs further improvement and optimization for the formation of deeper macroporous layers, its potential for the formation of supported and free-standing macroporous silicon membranes on p-type wafers has been demonstrated.

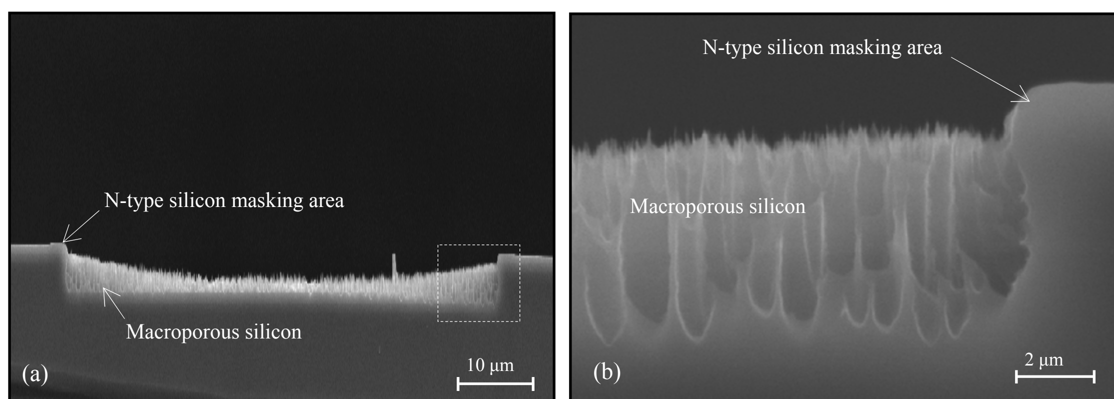


Fig. III.1.4: *SEM images of the cross-section of a confined macroporous silicon membrane. The masking material used was n-type Si created through P implantation. The trenches at the sides of the membrane are not formed. The area selected by the square in picture (a) is magnified in (b).*

C. Microfluidic flow sensor based on porous silicon technology

D. N. Pagonis, A. Petropoulos, G. Kaltsas, A. Tserepi and A. G. Nassiopoulou

This work concerns the fabrication, modelling and testing of a novel microfluidic flow sensor based on a microchannel capped with a porous silicon membrane, on top of which the sensor active elements are integrated. The microchannel is formed through a two-step anodization process. In the first step a mesoporous silicon layer is formed on a lithographically defined area, while in the second step a channel is formed underneath the porous layer by electropolishing. The channel is buried into bulk silicon and capped with a free-standing porous silicon layer, which is co-planar with the Si substrate. The developed technology shows important advantages compared to other existing techniques, which are: a) the simplicity and low cost of the process (formation of a self-sealed, buried microchannel in a single two-step electrochemical process) and b) the compatibility of the process with integrated circuit fabrication processing, which allows integration of the device on the same chip with silicon electronics.

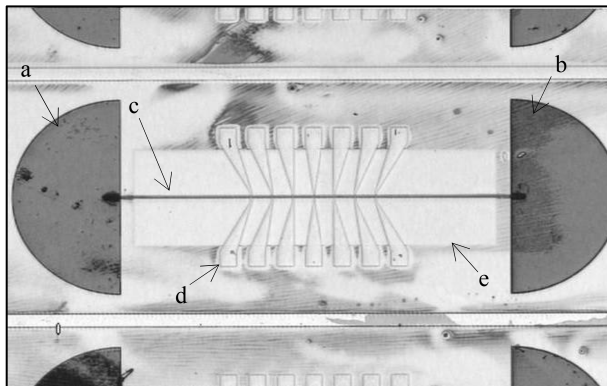


Fig. III.1.5: *Top-view optical picture of the formed microfluidic sensor, where we identify the inlet (a) and outlet (b) semi-circular reservoirs of the device, the buried microchannel (c) and the integrated sensing elements (d). The passivation layer on top of the active area of the device is also seen (e).*

Investigation of the device operation has been performed through appropriate simulations. Experimental testing of the prototype has been performed, after mounting the device in an appropriate package.

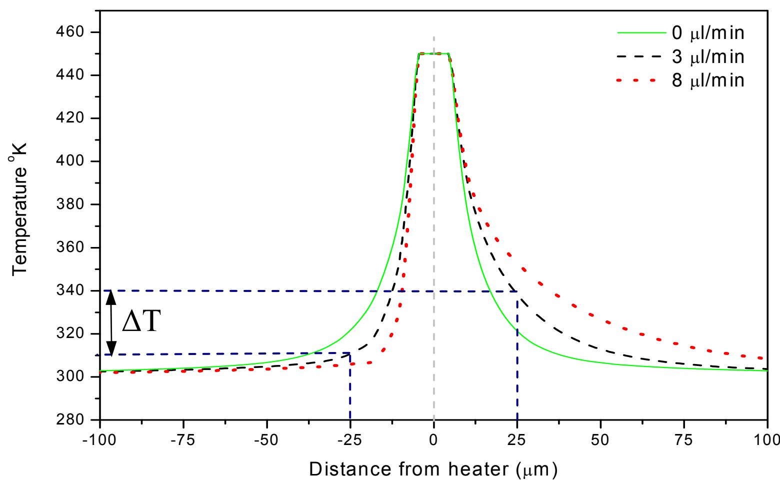


Fig. III.1.6: *Typical simulation results of the temperature distribution on the porous silicon capping layer of the microchannel. A symmetrical distribution is obtained with respect to the centre of the heater (dashed vertical line), when no flow is assumed, as expected. On the contrary, under flow, a significant asymmetry is observed due to convective heat transfer. The resulting temperature difference (ΔT) between two symmetrical points, situated 25 μm away from the heater has been indicated for a flow of 3 μL/min. The larger the flow rate is, the greater is the departure from symmetry.*

In order to demonstrate the functionality of the device, liquid was pumped into the inlet of the device at various flow rates from 2 μl/min up to 60 μl/min, while optical pictures under a microscope were taken. The liquid debouched successfully only through the outlet of the device, thus, the microchannel is empty from any remnants which could have been created from the electropolishing stage of the microchannel formation process, while the capping layer has sufficient mechanical stability to withstand the pressure induced by the flow of the liquid. Further experimental characterization of the device operation is in progress.

D. Copper wires within macroporous Silicon layers

F. Zacharatos and A. G. Nassiopoulou

In the present work a novel technique concerning the development of copper wires in a macroporous silicon template is demonstrated. Electrochemistry has been utilized for both the fabrication of the macroporous silicon films and the copper deposition inside the pores.

The starting materials in this investigation were p-type, 6-8Ω.cm silicon wafers. Their surface was pre-patterned properly, since the resulting structure was intended to have a specific arrangement. The pre-patterning process includes photo-lithographic as well as silicon wet etching steps. The result of this procedure is the formation of pore initiation pits that resemble inverted pyramids and form regular arrays on the substrate. The succeeding electrochemical anodization lead to the formation of regularly ordered arrays of pores with a diameter of 4-8μm (fig. III.1.7a) The thickness of the porous layer ranged from 30 to 120μm (fig. III.1.7b). By optimizing the electrochemical conditions, pores with even greater aspect ratios can be achieved.

The successful fabrication of the macropore arrays is followed by a thin thermal oxide development and a second electrochemical process. During this procedure, whose duration may exceed 120 min, copper particles are forced to deposit on the pore walls (fig. III.1.8a) and inside the macroporous film, until the pores are completely filled. The efficiency of the electrolytic solution is very sensitive in terms of composition and pH. The implementation of appropriate conditions followed by annealing, result in the development of homogeneous and consistent 50μm long copper wires (fig III.1.8b).

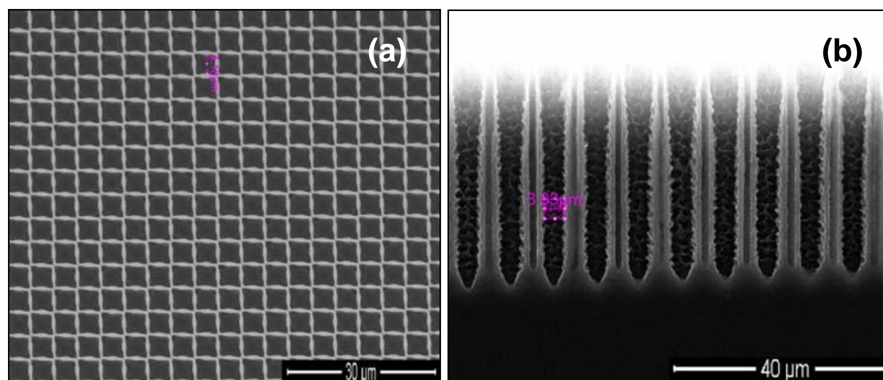


Fig. III.1.7: *SEM image of a typical ordered Macroporous Silicon layer formed on a p-type Si wafer. In (a) a top and in (b) a cross-sectional view of a sample with 50μm long pores are shown.*

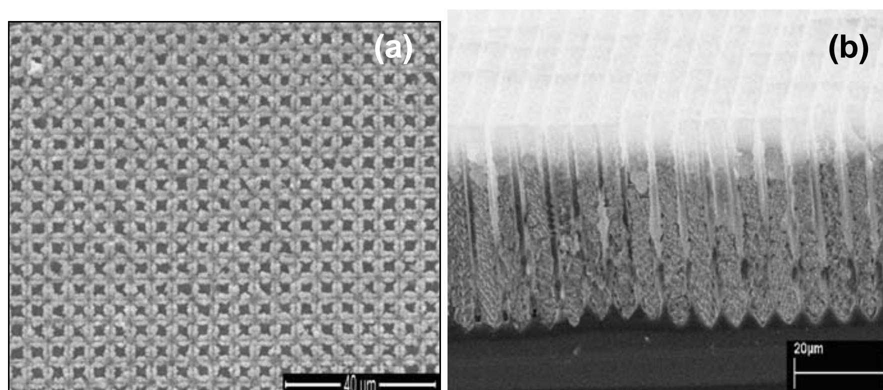


Fig. III.1.8: *SEM image of the samples after Cu deposition. (a) On the surface copper particles cover the pore walls (b) In cross-section, 50μm long copper wires are observed.*

PROJECT OUTPUT in 2006

Publication in Refereed Journals

1. “Design and simulation of integrated inductors on porous silicon in CMOS-compatible processes”, H. Conopanagos and A. G. Nassiopoulou, Sol. St. Electronics, vol. 50 (7-8) 1283 (2006)
2. “Free-standing macroporous silicon membranes over a large cavity for filtering and lab-on-chip applications", D. N. Pagonis and A. G. Nassiopoulou, Microelectronic Engin. 83, 1421–1425 (2006)

Papers in Conference Proceedings

1. “Porous silicon for sensors and on-chip integration of RF components”, A. G. Nassiopoulou (invited paper), Proceedings of the 4th International Conference on Microelectronics, Devices and Materials, Slovenia 13-15 September 2006, p. 33
2. “Integrated inductors on porous silicon”, H. Contopanagos, A. G. Nassiopoulou, Proceedings of the 5th International Conference on Porous Semiconductors-Science and Technology (PSST), Sitges-Barcelona, 12-17 March, 2006
3. “Local formation of suspended macroporous Si layers on a Si substrate”, D.N. Pagonis, A.G. Nassiopoulou, Proceedings of the 5th International Conference on Porous Semiconductors-Science and Technology (PSST), Sitges-Barcelona, 12-17 March, 2006
4. “Novel microfluidic flow sensor fabricated using porous silicon technology”, D.N. Pagonis, A. Petropoulos, G. Kaltsas, A.G. Nassiopoulou, A. Tserepi, Proceedings of the 5th International Conference on Porous Semiconductors-Science and Technology (PSST), Sitges-Barcelona, 12-17 March, 2006
5. “A silicon integrated thermal liquid flow sensor on porous silicon micro-hotplate”, D. N. Pagonis, G. Kaltsas and A. G. Nassiopoulou, Proceedings of the 20th Eurosensors Conference, Göteborg, Sweden, 17-20 September 2006

Conference Presentations

1. “Copper wire fabrication in macroporous Silicon templates”, F. Zacharatos and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science , Patras, Greece, September 2006
2. “Fabrication of SiO_2 quantum dots on Si Substrate through porous aloumina mask”, V. Gianneta, M. Kokonou and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science , Patras, Greece, September 2006
3. “Porous anodic aloumina on Si as a template for Au nanowires fabrication”, V. Gianneta and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science , Patras, Greece, September 2006
4. “A novel microfabrication technology for plastic sensors formation”, I. K. Tsougeni , G. Kaltsas, A. Petropoulos , P. Asimakopoulos, D. N. Pagonis and A. G. Nasiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science , Patras, Greece, September 2006
5. “Integrated microflow sensor based on porous silicon technology”, D. N. Pagonis,A. Petropoulos,G. Kaltsas and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science , Patras, Greece, September 2006

Invited Talks

1. “Porous silicon for on-chip integration”, A. G. Nassiopoulou (Tutorial), PSST-2006, Barcelona-Spain, 12-17 March 2006
2. “Porous silicon for sensors and on-chip integration of RF components”, A. G. Nassiopoulou (Invited Talk), 42th International Conference on Microelectronics, Devices and Materials and Workshop on MEMs, NEMs, September 13-15, 2006, Slovenia

Organisation of Conferences, Symposia, Workshops

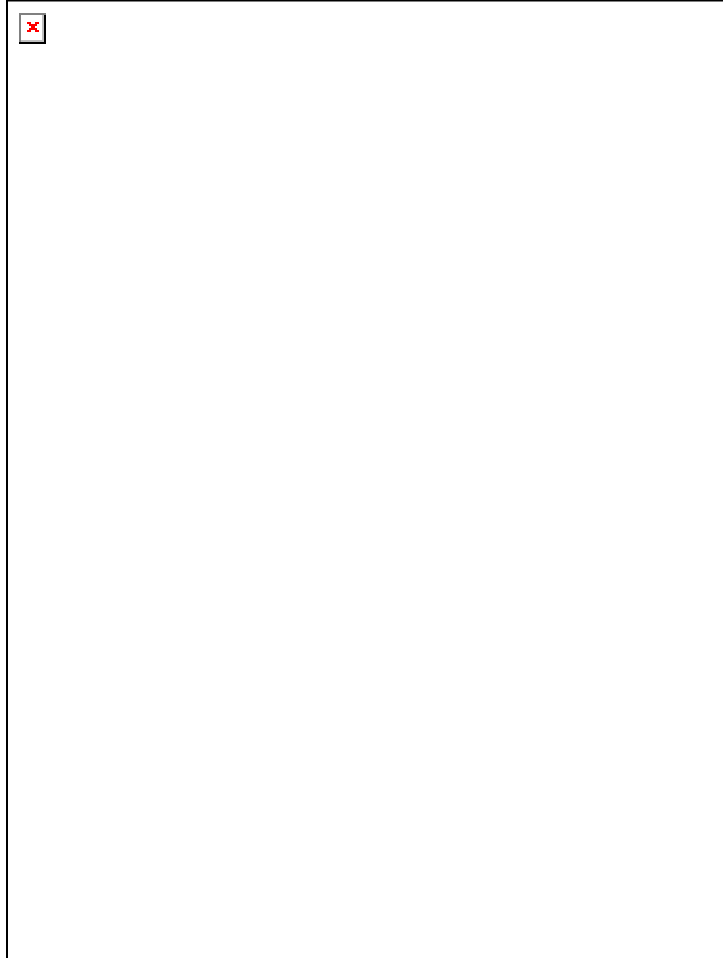
1. PSST - 5th International Conference on Porous Semiconductors-Science and Technology, Sitges-Barcelona, 12-17 March, 2006, Chairpersons: V. Parkhutik, L. Canham, A. G. Nassiopoulou, M. Sailor, Edition of Proceedings, Special issue of Physica Status Solidi, Physica Status Solidi

Patent filing

1. “Low power silicon thermal sensors and microfluidic devices based on the use of porous silicon sealed air cavity or microchannel technology”, PCT patent, International publication, No W003/062134, Inter. Publ. date: 31/7/2003, Filing in USA, Japan Europe, China

DISTINCTION

Cover page of Physica Status Solidi, May 2007



Cover picture story pss (a) 204-5**: Integrated Inductors on Porous Silicon**

The cover picture illustrates the effective use of a thick porous silicon layer as an integrated micro-plate for RF isolation on a silicon substrate, proposed by Harry Contopanagos and Androula Nassiopoulou in their Original Paper [1] in the current issue. What is plotted is the magnitude of the current distribution on the metallization and on a screen 50μm underneath the bottom oxide layer of a 2-metal integrated CMOS-compatible inductor on bulk silicon (left) and on a 50 μm thick porous silicon layer (right) for a frequency of 2.5 GHz.

[1] H. Contopanagos and A. Nassiopoulou, phys. Stat. sol. (a) 204 No5, 1454-1458 (2007)