# PROJECT III.4

## CIRCUITS & DEVICES FOR OPTOELECTRONIC INTERCONNECTIONS

**Project Leader: G. Halkias** (until July 2007)

**Key Researchers:** G. Halkias, S. G. Katsafouros, E.D. Kyriakis-Bitzaros

**PhD Candidates:** K. Minoglou

**Research Associates:** E. Grivas, P. Robogiannakis

**Objectives**

The main objective of the project is the development of the technologies for future high-density and high-speed optoelectronic interconnections. In order to accomplish this objective the additional specific targets of optoelectronic device modeling and simulation, implementation of optoelectronic technology in spacecraft environment as well as packaging in terms of photonic link integration above CMOS integrated circuits have been identified.

**Funding**

- EU- IST PICMOS, 2004-2007
- ESA- Multigigabit optical backplane for space applications, 2004-2006

### RESEARCH RESULTS

#### A. Development of a model for simulating Vertical Cavity Surface Emitting Lasers (VCSELs) and driving circuit topologies

Motivated by the fact that the ability to model VCSEL optical behaviour is critical to the design and analysis of optoelectronic micro-systems, we developed a model, which combines the non-linear behaviour of the input parasitics with the intrinsic fundamental device carrier and photon rate equations. The complete model for the VCSEL is implemented by means of equivalent circuits for the fundamental device rate equations, the thermal effects, the non-linear gain and transparency number functions and the input parasitic elements. A systematic methodology for the model parameter extraction from dc and ac, electrical and optical measurements is developed. Model parameters are divided into three distinct groups and their determination is achieved by a three-step procedure. The first two steps of the procedure focus on the parameters of the VCSEL's input and use the dc I-L-V characteristics at different temperatures and the $S_{11}$ parameters, while the third one is based on $S_{21}$ parameter measurements at different bias currents and taking into account the already defined model parameters extracts the remaining ones which mainly refer to the optical output. The parameter extraction procedure is proved to be very fast while it preserves adequate accuracy. As shown in Fig.III.4.1 a and b, simulation results using the proposed model, is compared with the experimental measurements and present satisfactory agreement. Also, the transient response of the optical signal of a VCSEL is depicted in the form of eye diagrams at different frequencies using voltage pulse drivers in Fig. III.4.2 a and b.

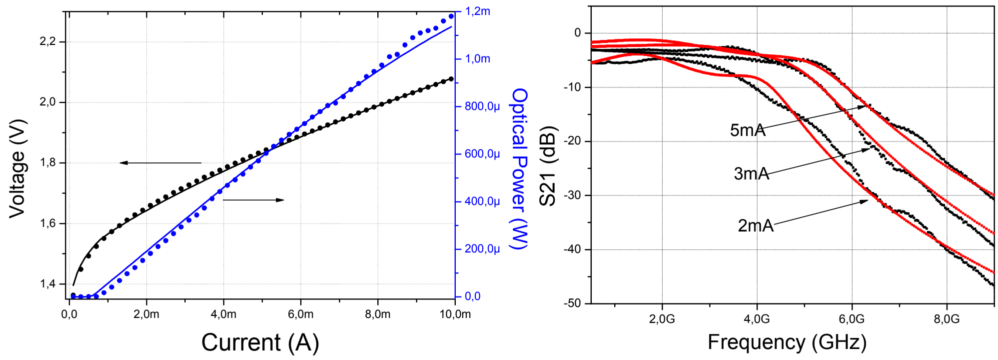
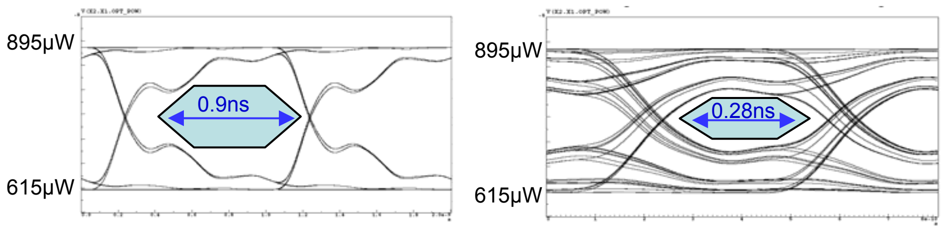



***Fig. III.4.1:*** *(a) Measurements (dots) and simulations (continuous line)of DC I-V and I-L and (b) measured values (black line) and simulated (red line) $S_{21}$ optical response at different bias currents*




(a) 1Gb/s (b) 2.5 Gb/s

***Fig. III.4.2:*** *Simulated eye diagrams with voltage pulse driving at different frequencies*

## B. Multigigabit optical backplane for space applications

During the Extension phase of the project the most relevant protocols for the selected architecture were investigated and the appropriate recommendations were made. The different types of MAC protocols examined provide different characteristics in terms of network throughput, latency and bandwidth utilization. Moreover, the performance of each one is strongly related to the type of traffic it serves. As such, an effort to come-up with a type of protocol for use with the backplane proposed seems to be pointless. In contrast, several features of the protocols from these categories could be combined into a single protocol that provides different classes of services.

**Random MAC**: This class of protocols is the simplest one. There is no arbitration mechanism to allocate network resources and nodes comprising the network are in a continuous contention for resources. Packet collisions may happen at any time and when one occurs, packets have to be retransmitted. A back-off mechanism is often used to reduce the possibility of a collision between retransmitted packets. Random MAC protocols are very popular due to their simplicity that makes them a cost effective solution. Their theoretical performance is very poor, however, in practice they, surprisingly, seem to work. The most popular implementation of random protocols is the ALOHA protocol, while the Ethernet protocol was based on it.

**Preallocation MAC**: As its name implies, this class of protocols allocates network resources in advance of network utilization. The allocation is performed in a collision free manner, so that data is guaranteed to be transmitted error free. Point-to-point links is an example of a preallocation MAC protocol, where such a link is dedicated to the communication of two nodes. When multiple nodes share a common link (or part of it) Time Division Multiple Access (TDMA) may be employed. In such a scheme every time slot is preallocated to a pair of nodes. The set of every possible combination between pairs of nodes forms a cycle, which is repeated forever. These protocols offer great performance in terms of throughput at medium to high loads, but experience low network utilization at low traffic. The average packet delay is independent of the network load, but increases as the number of nodes increases. At a first glance it can be approximated as half the cycle time.

**Reservation MAC**: This class of protocols is the most sophisticated. It employs one or more control channels that are being used for resource reservation prior to data transmission. In that way data packet collisions are being prevented, while resources can be dynamically allocated to nodes leading to performance improvement at any possible type of traffic. Moreover, reservation protocols can support different arbitration mechanisms, so that they can offer a variety of Quality of Service (QoS). All these benefits provided by these protocols are in expense of an increased cost since the allocation of resources (wavelengths and slots) of the network should be calculated by a dedicated scheduler.
Random MAC protocols provide better performance in terms of latency and acceptable throughput when traffic is relatively low. They are suitable for computer networks, where data appear in short bursts and network resources remain unutilized most of the time. Pre-allocation MAC protocols offer guaranteed throughput under any type of traffic. Latency is strongly related to the number of nodes comprising the network. Finally, reservation MAC protocols offer better and more balanced performance, but at an increased cost and hardware complexity.

## C. Heterogeneous integration of optical interconnects onto CMOS ICs

The ever decreasing transistor size has already begun to transfer the bottleneck of high-speed circuit performance from the active devices to the electrical interconnect. The employment of a photonic layer above CMOS integrated circuits (ICs) has been proposed as an alternative solution for the global interconnection regime. Photonic dies with fully integrated optical paths-sources and detectors coupled to waveguides are bonded onto a CMOS integrated circuit (IC) using a metallic bonding technique. The proposed approach utilizes a thin multilayer structure of the Au-20Sn eutectic alloy along with a thin starting layer of rare earth Gd and contains versatile structures for passive alignment. Its main advantage is the fact that it accomplishes mechanical bonding and electrical connectivity in a single step. The proposed approach resembles flip-chip approach, but the solder volume and size are considerably lower making it appropriate for high-density integration. Pattern uniformity, limited alloy spreading and contact resistance in the mΩ range across a 4-inch wafer has been verified. Fig. III.4.3 shows a patterned 4in wafer where convex structures are formed to match with the corresponding concave structures patterned on the dies. Fig. III.4.4 a and b present the patterns on wafer and on dies that are used for the metallic interconnect test measurements, while Fig. III.4.4c shows very good die-to-wafer achieved alignment. This project is executed in collaboration with IMEC, Belgium, ST, CEA, CNRS-FMNT, France, and TUE, Holland, in the framework of the European project PICMOS.

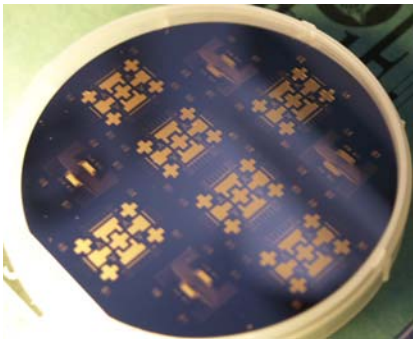
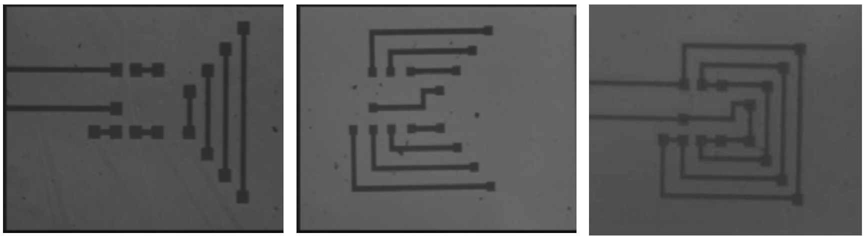


***Fig. III.4.3:*** *Four-inch wafer with metallic lines and convex features (crosses) for alignment on it.*



(a) (b) (c)

***Fig.III.4. 4:*** *Appropriate patterns on the wafer (a), the dies (b), so that they can be used for the electrical tests after the bonding (c).*

# PROJECT OUTPUT IN 2006

### Publications in Conference Proceedings

1. K.Minoglou, E.D. Kyriakis-Bitzaros, D. Syvridis, G. Halkias, “Input and Intrinsic Device Modeling of VCSELs”, book of abstracts of IWCE 2006, pp.327-328 (presented in IWCE 2006, International Workshop on Computational Electronics, May 25-27, Vienna, Austria)
2. K.Minoglou,, E.D. Kyriakis-Bitzaros, D. Syvridis, A. Arapoyanni, G. Halkias, “VCSELs modeling and Simulation”, proceedings of PRIME 2006, pp.201-204 (presented in PRIME 2006, June 12-15, Otranto, Italy)
3. E. Grivas, E.D. Kyriakis-Bitzaros, G. Halkias, S. Katsafouros, G. Morthier, P. Dumon, R. Baets, T. Farrell, N. Ryan, I. McKenzie, and E. Armadillo, “WDM Based Multigigabit Optical Backplane for On-Board Applications”, Int. Conference on Space Optics, 27-30 June 2006, ESA/ESTEC, Nordwijk, The Netherlands
4. P. Robogiannakis, E. D. Kyriakis-Bitzaros, K. Minoglou, S. Katsafouros, A. Kostopoulos, G. Konstantinidis and G. Halkias, “Heterogeneous integration technique of optoelectronic dies to CMOS circuits via metallic bonding” , ESTC 2006, 1st Electronics Systemintegration Technology Conference, Dresden, Germany, 5-7 September 2006
5. E.D. Kyriakis-Bitzaros, E. Grivas, G. Halkias, S. Katsafouros, P. Dumon, G. Morthier, R. Baets, T. Farell, N. Ryan, I. McKenzie, and E. Armadillo, “A WDM Optical Backplane with AWG Based Passive Routing”, Photonics in Switching Conference, 16-18 Oct. 2006,Heraklion, Crete, Greece

### Conference Presentations

1. “A WDM Optical Backplane with AWG Based Passive Routing”, E.D. Kyriakis-Bitzaros, E. Grivas, G. Halkias, S. Katsafouros, P. Dumon, G. Morthier, R. Baets, T. Farell, N. Ryan, I. McKenzie, and E. Armadillo, Photonics in Switching Conference, 16-18 Oct. 2006,Heraklion, Crete, Greece.
2. “WDM Based Multigigabit Optical Backplane for On-Board Applications”, E. Grivas, E.D. Kyriakis-Bitzaros, G. Halkias, S. Katsafouros, G. Morthier, P. Dumon, R. Baets, T. Farrell, N. Ryan, I. McKenzie, and E. Armadillo, Int. Conference on Space Optics, 27-30 June 2006, ESA/ESTEC, Nordwijk, The Netherlands
3. “Heterogeneous integration technique of optoelectronic dies to CMOS circuits via metallic bonding”, P. Robogiannakis, E. D. Kyriakis-Bitzaros, K. Minoglou, S. Katsafouros, A. Kostopoulos, G. Konstantinidis and G. Halkias, ESTC 2006, 1st Electronics Systemintegration Technology Conference, Dresden, Germany, 5-7 September 2006.
4. “Input and Intrinsic Device Modeling of VCSELs”, K.Minoglou, E.D. Kyriakis-Bitzaros, D. Syvridis, G. Halkias, book of abstracts of IWCE 2006, pp.327-328 (presented in IWCE 2006, International Workshop on Computational Electronics, May 25-27, Vienna, Austria).