Project III. 5

THIN FILM DEVICES for LARGE AREA ELECTRONICS

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- GSRT bilateral project Greece-Serbia, Polysilicon TFT reliability, 1/11/2004 – 31/10/2006.

Objectives

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors fabricated in such films. Specifically, the targets are:

- Investigation of the influence of the polysilicon crystallization technique and film thickness on TFT performance, defect densities and degradation for ELA technology optimization.
- Evaluation of device parameter (a) hot carrier and (b) irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films.
- Investigation of effects of variations in TFT structure and fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Evaluation of bias stress-induced instabilities in solid phase crystallized (SPC) TFTs.

RESEARCH RESULTS

A. Characterization of ELA TFTs of varying technologies and structures

The characterization of TFTs made in sequentially laterally solidified (SLS) ELA polysilicon films has proceeded with the investigation of both different polysilicon crystallization technologies and different device structures. Advanced variations of the SLS ELA technique have been investigated and compared to the original directional technique. Furthermore, the performance parameters and characteristics of TFTs having top gate, bottom gate and double gate structures have been extracted and useful information for technology development has been obtained.

TFTs in “directional” SLS ELA films have very elongated grains along a preferred direction. Advanced variations of the SLS ELA technique, utilizing laser exposure through masks with many parallel slits, have been introduced to increase throughput, resulting in so-called 2-shot, 2^N-shot and M×N polysilicon films which have engineered rectangular grain shapes; a preferred direction still exists along the larger grain dimension but vertical boundaries also exist. TFTs in these advanced films have been characterized; the intragrain material quality was found to be higher for 2^N-shot devices, as evidenced by a lower grain boundary trap density, extracted following a Levinson analysis. The average device parameters, for top gate TFTs with various polysilicon film crystallization technologies, are summarized in the following table:

Crystallization technology	Field Effect Mobility, μ ($cm^2/V \cdot sec$)	Threshold Voltage, V_{th} (V)	Subthreshold Slope, ***S*** (mV/dec)	Grain Boundary Trap Density, N_t (cm^{-2})
directional	320	-1.1	130	4.9×10^{11}
2-shot	282	-1.8	390	6.5×10^{11}
2^N-shot	188	0.2	160	3.8×10^{11}
M×N	289	-0.2	170	3.4×10^{11}

In polysilicon TFTs localized traps near the drain augment free carrier generation-recombination rates, giving rise to parasitic bipolar effects through the back-interface area that enhance the drain current. In directional TFTs no boundaries intersect the current; only a low density of recombination centers exists. The parasitic bipolar action by transport of generated minority carriers is thus expected to be enhanced, yielding an additional excess I_{DS}. This is confirmed in Figure III.5.1, which shows the output I_{DS}-V_{DS} characteristics for TFTs in 2^N-shot, 2-shot or directional polysilicon films; directional TFTs exhibit a higher excess drain current. It is thus determined that the susceptibility to drain current avalanche effects is lower for TFTs in advanced 2^N-shot polysilicon films.

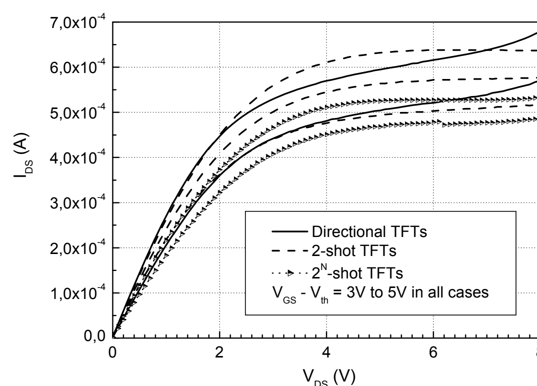

Fig. III.5.1: *Output characteristics of TFTs in 2^N-shot, 2-shot or directional polysilicon films.*

ELA TFTs oriented along a non-preferred direction are also under investigation, typically yielding significantly lower carrier mobilities and higher trap state densities. Moreover, in addition to advances in polysilicon crystallization technology, variations in TFT achitecture also offer enhanced performance characteristics and flexibility for the design of TFT-based circuits. TFTs having bottom gate (BG) and double gate (DG) structure have been investigated, as well as top gate (TG) ones. Double gate TFTs (top and bottom gate lengths L_t, L_b) offer the possibility of operation either from the top or from the bottom gate, with the opposing gate held at a given bias. As seen in Figure III.5.2, for both operation modes the transfer characteristics exhibit higher drain current for smaller L_b. This indicates that the presence of the back gate, while beneficial in terms of threshold voltage control, avalanche suppression or other electrical

aspects, allowing more flexibility in circuit design, has to be optimized to avoid deleterious effects on the DG TFT characteristics due to inferior bottom interface quality.

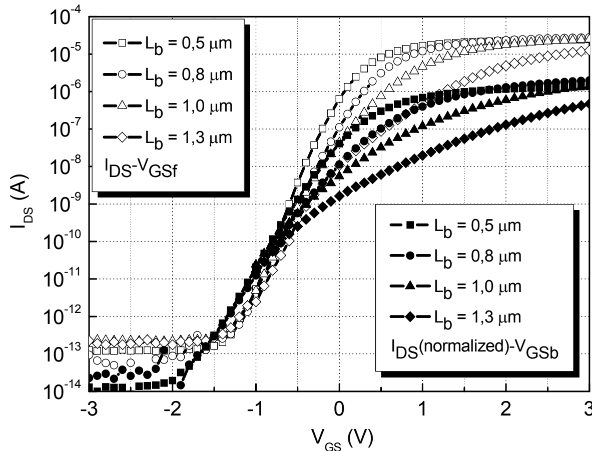

Fig. III.5.2: *DG TFT I_{DS}-V_{GSf} (for V_{GSb} = 0 V) and I_{DS}-V_{GSb} (for V_{GSf} = 0 V) characteristics, at V_{DS} = 0.1 V.*

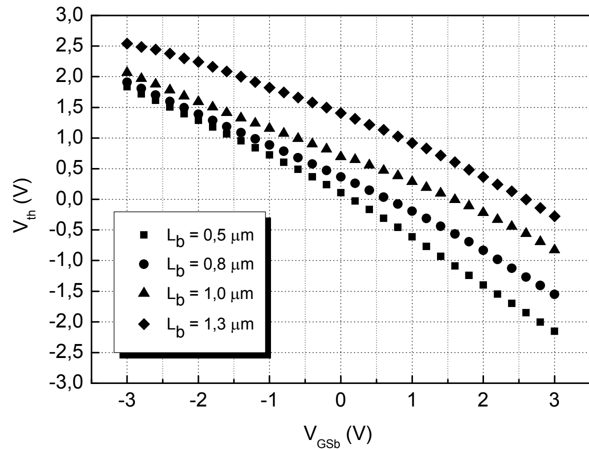

Fig. III.5.3: *V_{th} of DG TFTs for front operation against back gate bias, for TFTs with L_f = 1.6 μm and L_b ranging from 0.5 μm to 1.3 μm.*

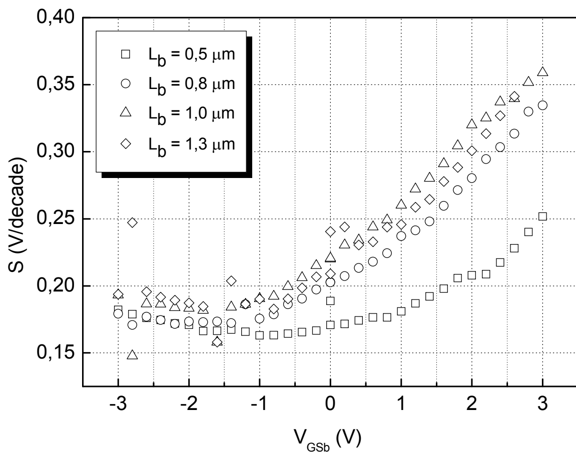

Fig. III.5.4: *Swing of DG TFTs for front operation against back gate bias, for TFTs with L_f = 1.6 μm and L_b ranging from 0.5 μm to 1.3 μm.*

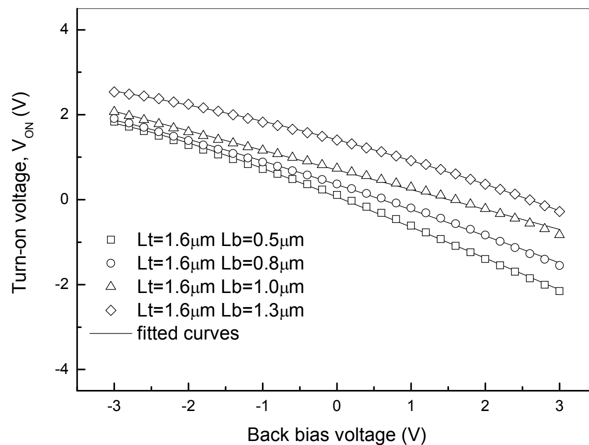

Fig. III.5.5: *V_{th} data and model fit against back gate bias voltage for asymmetric double gate TFTs (W = 8 μm) with various L_t/L_b ratios.*

The continuous V_{th} shift (Fig. III.5.3), without a plateau, indicates full depletion of the polysilicon films. For increasingly negative values of V_{GSb}, the values of V_{th} and, even more, of ***S*** (Fig. III.5.4) tend to cluster together. This is ascribed to the fact that the top operation of the DG TFT, due to the asymmetry in the values of L_f and L_b, involves series double gate and top gate TFTs. As the bottom channel contribution is reduced and eventually cut off, the drain current flows solely from the top channel and the ***S*** and V_{th} values, which mostly depend on the interface quality, settle towards those of a top gate transistor, even in the double gate area. An effort to model V_{th} for an asymmetric DG TFT is in progress, with preliminary results predicting its dependence on L_b/L_t (Fig. III.5.5).

A process flow for TFTs on oxidized silicon substrates has been developed and the first devices have been fabricated at IMEL, either with SLS ELA crystallization at Sharp or furnace anneal at IMEL. Preliminary results indicate good quality devices. Process variations, like novel gate dielectrics, will be introduced in TFTs still in the fabrication process at IMEL. This will allow the investigation of the effects of these variations on SLS ELA TFT performance, prior to their being tested by the industry.

B. Hot carrier stress investigation

TFT degradation under hot carrier stress (HCS) was investigated for devices fabricated in advanced 2^N-shot polysilicon films, as compared to directional ones. Figure III.5.6 shows the V_{th} and ***S*** evolution with stress time for a HCS condition (V_{GS}, V_{DS}) = (5 V, 10 V), for TFTs in 2^6-shot polysilicon films or in directional ones, while in figure 7 the evolution of the maximum transconductance $G_{m,max}$ is shown. A "minimal" stress condition of (V_{GS}, V_{DS}) = (5 V, 5 V) is shown to only have a negligible effect on all parameters for TFTs in both kinds of films.

There is a V_{th} shift due to the application of the (5 V, 10 V) stress, which is positive for 2^6-shot polysilicon TFTs and negative for directional ones. TFT degradation depends on carrier injection in the oxide, on trapping at interface states and on trapping at states at polysilicon grain boundaries. In directional material the last mechanism, which would introduce positive V_{th} shift, is less probable, as no boundaries vertical to the current flow exist. It is thus observed that in directional TFTs, under this stress condition, where we have predominantly hole injection, V_{th} exhibits a negative shift. In 2^N-shot material all three mechanisms contribute and the slight positive V_{th} shift may be attributed to the influence of electron trapping in the vertical grain boundaries.

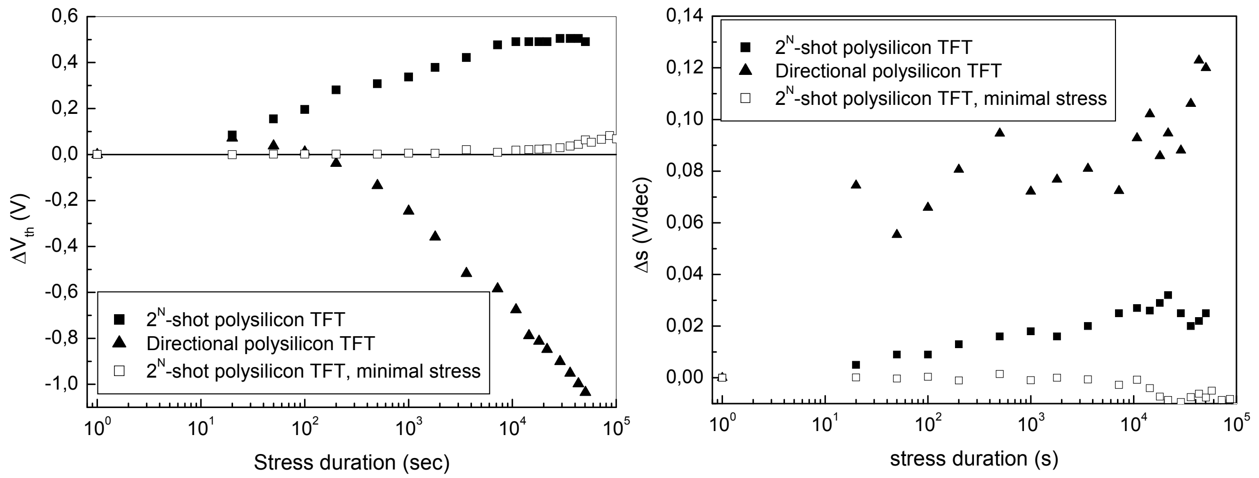

Fig. III.5.6: *Threshold voltage (left) and subthreshold swing (right) variation for SLS ELA TFTs in 2^N-shot or in directional polysilicon films, under a hot carrier stress (V_{GS}, V_{DS}) = (5 V, 10 V) or under a "minimal" stress of (5 V, 5 V).*

It is observed that the stress application results in a power-law time dependent $G_{m,max}$ degradation for TFTs in both 2^6-shot and in directional polysilicon films, while the ***S*** degradation is present in both cases but is worse for directional TFTs. It is known that ***S*** depends mostly on deep trapping at the polysilicon / SiO_2 interface and / or on intra-grain state generation, while $G_{m,max}$ depends mostly on interface state generation and / or on grain boundary trap generation (tail-states). These data thus support the existence of two different HCS degradation mechanisms for 2^6-shot or directional polysilicon TFTs.

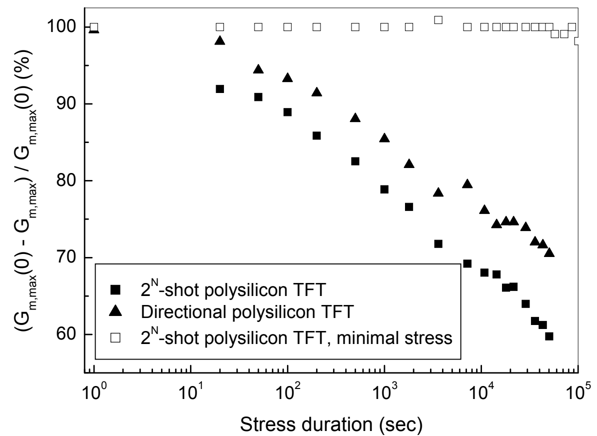

Fig. III.5.7: *Transconductance percentage variation for TFTs in 2^N-shot or in directional polysilicon films, under a hot carrier stress (V_{GS}, V_{DS}) = (5 V, 10 V) or under a "minimal" stress of (5 V, 5 V).*

C. Low temperature and transient current characterization

The inestigation of drain current transients, carried out in collaboration with the University of Athens, yields information critical for the assessment of the defectivity of polysilicon films obtained using various crystallization techniques. The obtained transients for SLS ELA TFTs are of the same order of magnitude at dark or under illumination and fall sharply at cryogenic temperatures, indicating polysilicon material of high crystalline quality with concentrations of generation-recombination centers much lower than those of standard SPC or ELA films. The device transient behavior temperature dependence, at dark or under illumination (Fig. III.5.8), suggests that the accountable mechanism cannot be attributed only to carrier trapping, but rather to a more complex mechanism involving carrier generation and recombination in the TFT body. It was determined that for ultra thin films the generation mechanism is different, possibly related to the proximity of the bottom interface, as evidenced by the data for 30 nm case not falling in line with those for 50 nm, 100 nm that show an exponential relationship between the generation lifetime and the activation energy (Fig. III.5.9). The dependence of thermally activated mechanisms on the film thickness suggests that the device operation is strongly related to the polycrystalline material properties.

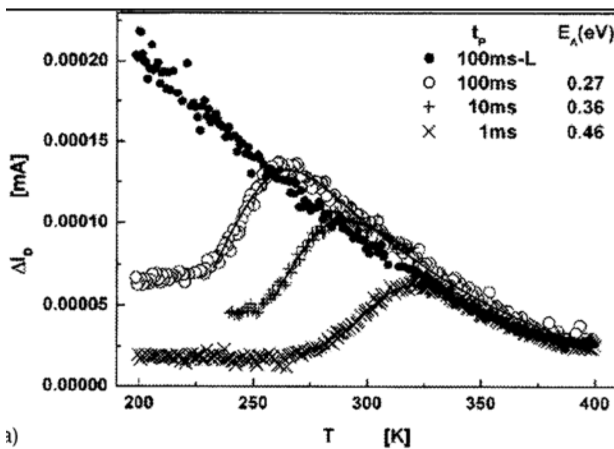

Fig. III.5.8: Transient amplitude dependence of 50 nm TFTs on temperature for various off pulses; filled circles are for measurement under illumination.

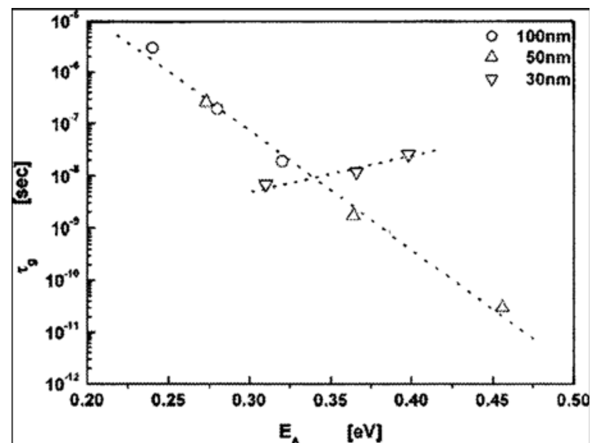

Fig. III.5.9: Carrier generation lifetime against the activation energy for directional TFTs having active layer thickness of 30, 50 or 100 nm.

D. Irradiation investigation

The degradation, under γ-irradiation, of the parameters of SLS ELA TFTs made in advanced “2-shot” polysilicon films has also been studied, in an investigation carried out in collaboration with the University of Nis, and compared with that for TFTs in directional films. It has been determined that 2-shot polysilicon TFTs are more resistant to γ-irradiation-induced degradation compared to directional ones. The characteristics of both 2-shot and directional ELA polysilicon TFTs for various irradiation doses, and anneals after the maximum dose, are shown in Figure III.5.10. The γ-irradiation of these TFTs results in positive oxide charge trapping, which induces negative V_{th} shifts. It is evident, from the larger negative shifts, that the irradiation-induced increases of the oxide trapped charges are smaller for TFTs fabricated in 2-shot polysilicon films. On the other hand, the subthreshold slope changes are similar, indicating similar interface degradation for TFTs of the two technologies.

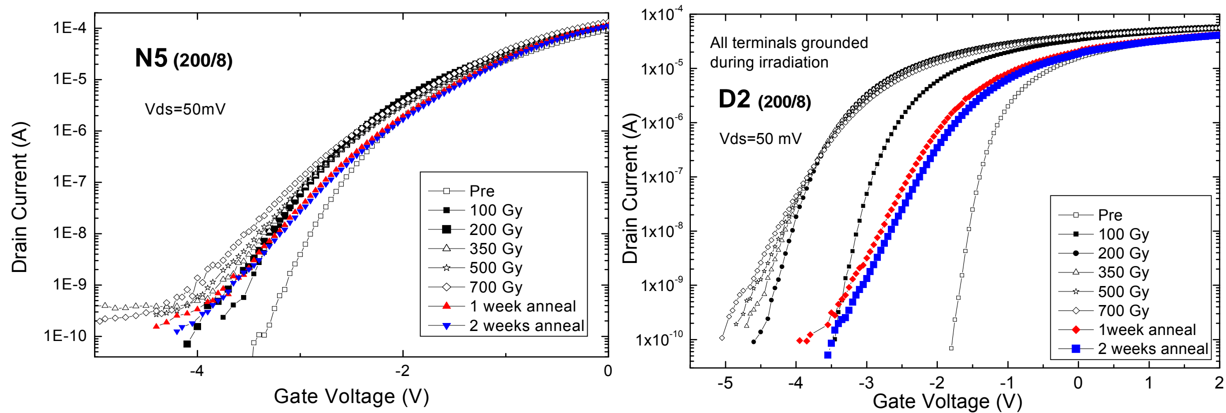

Fig. III.5.10: *Transfer characteristics I_{DS}–V_{GS} for 2-shot (left) and directional (right) SLS ELA polysilicon TFTs (W = 200 μm, L = 8 μm) for varying irradiation doses.*

E. Material characterization

The surface morphology and the grain structure of the polysilicon films depend on the crystallization technique. While directional films have a strongly preferential orientation, polysilicon films obtained with the advanced 2^N-shot technique exhibit engineered grain shapes with a high quality intragrain material, as shown, for comparison, in the SEM micrographs of Figure III.5.11. This difference in the material structure is reflected in TFT performance and reliability characteristics, as discussed in task 2. An investigation of the optical properties of advanced TFT gate dielectrics and of various SLS ELA polysilicon films, as a means for estimating their defectivity, is in progress.

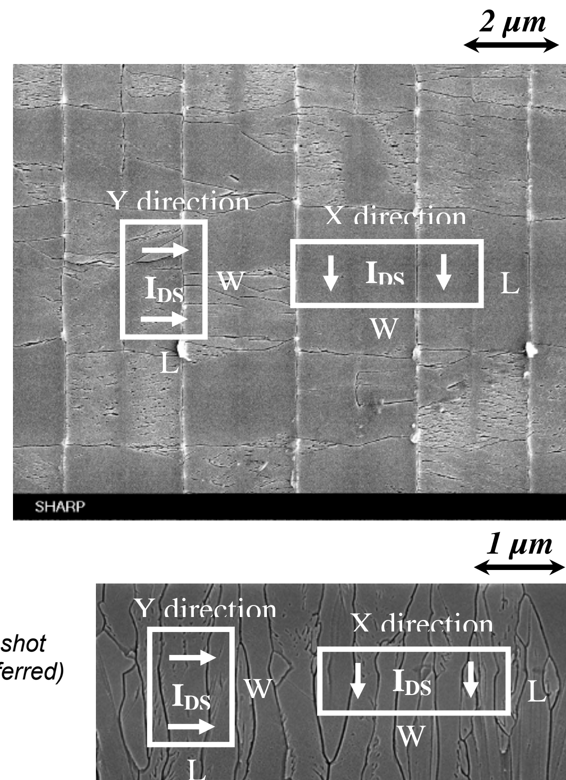

Fig. III.5.11: *SLS ELA polysilicon films obtained using 2^N-shot (top) or directional (bottom) techniques. Directions X (preferred) and Y are shown.*

PROJECT OUTPUT in 2006

Publications in International Journals and Reviews

1. Tsevas, S., M. Vasilopoulou, D.N. Kouvatsos, A. Speliotis and D. Niarchos, “Characteristics of MOS diodes using sputter-deposited tungsten or copper / tungsten films”, Microelectronic Engineering, 83 (4-9), 1434, April-September 2006.
2. Exarchos, M.A., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, “On the drain current overshoot transient in polycrystalline silicon transistors: The effect of hole generation mechanism”, Journal of Applied Physics, 99 (2), 024511, January 2006.
3. Kouvatsos, D.N., A.T. Voutsas, L. Michalas, F. Farmakis and G.J. Papaioannou, “Device degradation behavior and polysilicon film morphology of TFTs fabricated using advanced excimer laser lateral solidification techniques”, accepted to appear in Thin Solid Films.
4. Michalas, L., M. Exarchos, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, “An experimental study of the thermally activated processes in polycrystalline silicon thin film transistors”, accepted to appear in Microelectronics Reliability.
5. Kouvatsos, D.N., F.V. Farmakis, D.C. Moschou, G.P. Kontogiannopoulos, G.J. Papaioannou and A.T. Voutsas, “Characterization of double gate TFTs fabricated in advanced SLS ELA polycrystalline silicon films”, accepted to appear in Solid State Electronics.

Publications in Conference Proceedings

1. Farmakis, F.V., D.N. Kouvatsos, A.T. Voutsas, D.C. Moschou, G.P. Kontogiannopoulos and G.J. Papaioannou, “Front and back channel properties of asymmetrical double-gate polysilicon TFTs”, Thin Film Transistor Technologies VIII Symposium, Electrochemical Society Transactions 3 (8), 75, 2006.
2. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, “The role of grain boundaries in the performance of poly-Si TFTs”, Thin Film Transistor Technologies VIII Symposium, Electrochemical Society Transactions 3 (8), 87, 2006.
3. Michalas, L., M. Exarchos, G.J. Papaioannou, D. Kouvatsos and A. Voutsas, “Physics and electrical characterization of excimer laser crystallized polysilicon TFTs”, Proceedings of the 25th International IEEE Conference on Microelectronics (MIEL 2006), Nis, Serbia & Montenegro, May 2006.

Conference Presentations

1. Farmakis, F.V., D.N. Kouvatsos, A.T. Voutsas, D.C. Moschou, G.P. Kontogiannopoulos and G.J. Papaioannou, “Front and back channel properties of asymmetrical double-gate polysilicon TFTs”, The Electrochemical Society Extended Abstracts, vol. 2006-2, 2006 (210th Meeting of the Electrochemical Society, Cancun, Mexico, October 2006).
2. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, “The role of grain boundaries in the performance of poly-Si TFTs”, The Electrochemical Society Extended Abstracts, vol. 2006-2, 2006 (210th Meeting of the Electrochemical Society, Cancun, Mexico, October 2006).
3. Kouvatsos, D.N., A.T. Voutsas, L. Michalas and G.J. Papaioannou, “Device degradation behavior and polysilicon film morphology of TFTs fabricated using advanced excimer laser lateral solidification techniques”, European Materials Research Society Spring 2006 Meeting, Symposium I: Thin Film Materials for Large Area Electronics, Nice, France, May 2006.

Conference Participation

Participation in the following conferences:

1. Spring 2006 European Materials Research Society Meeting, Nice, France, May 2006
2. 25th International IEEE Conference on Microelectronics (MIEL 2006), Nis, Serbia & Montenegro, May 2006
3. 210th Meeting of the Electrochemical Society, Cancun, Mexico, October 2006

Organization of Conferences, Workshops and Project Meetings

Reviewer – Member of the Technical Programme Subcommittee of the 25th International IEEE Conference on Microelectronics (MIEL 2006), Nis, Serbia & Montenegro, May 2006.