Project II.2

NANOCRYSTAL MEMORIES

Project leader: Dr P.Normand

Key researchers: Dr P. Normand, Dr V. Ioannou-Sougleridis
Collaborating researchers: Dr. P. Argitis, Dr. M. Chatzichristidi, Dr. J. Raptis
Post-doctoral: Dr V. Vamvakas
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Objectives

- To develop novel high-throughput synthesis routes and techniques for creating nanostructured materials in dielectrics, such as Si nanocrystals in SiO_2 films by low-energy ion-beam-synthesis.
- To investigate the structural and electrical properties of the generated nanostructured materials and demonstrate material characteristics enabling the development of low-voltage high-density memory devices.
- To realize and evaluate nanostructure-based-memory devices and assess the manufacturability of the developed nanofabrication routes in an industrial environment.

Funding

- NEON, Nanocrystals for Electronic Applications, EU GROWTH GRD1, No 25619
- Bilateral French-Greek Project, Si-Nanocrystal Synthesis by Plasma-Immersion Ion-Implantation for Non-Volatile Memory Applications, ΕΠΑΝ. Μ.4.3.6.1Ε.

Activities

By associating the finite-size effects of nanocrystals and the benefits of a stored charge distribution, the nanocrystal memories (NCMs) have the potential to fulfill the stringent requirements of non-volatile memory cell downscaling. Our activities in this area started in 1996 through the development of the low-energy ion-beam-synthesis (LE-IBS) technique for producing nanocrystals in thin gate dielectrics. This activity was supported by the EU project, FASEM (1997-2000). LE-IBS development with target the realization of manufactory non-volatile NCMs has been conducted within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last four years for developing novel NCMs alternatives including, (a) Memory devices by Si^+ irradiation through poly-Si/SiO_2 gate stack in collaboration with FZR and ZMD Dresden, (b) Memory devices using Ge nanocrystals produced by MBE and rapid-thermal processing in collaboration with Aarhus Univ., (c) hybrid silicon-organic and SiGe-organic memories in collaboration with Durham Univ.; this last activity was conducted within the framework of the EU IST-FET project, FRACTURE (2001-2003).

In 2006, our main activities were focused on the following four tasks:

1. Block-copolymer-assisted-nanostructure fabrication for memory applications
2. Ge nanocrystals in high-k dielectrics obtained by low-energy ion-beam-synthesis
3. Channel edge effects in shallow-trench-isolated nanocrystal memories
4. Oxide/nitride/oxide (ONO) dielectric stacks with Si nanocrystals embedded in nitride

During 2006, activities aiming at the development of a Si-NC synthesis route based on plasma-immersion ion-implantation (PIII) in collaboration with CEMES/CNRS and one French SME (Ion Beam Services) were initiated. Our group was also involved in research activities conducted at NTUA (Prof. D. Tsoukalas) regarding NCM radiation hardness.

Specific targets for 2007 include: (a) Fabrication of nanostructures by block-copolymer nanopatterning in collaboration with project I.1, (b) formation of ONO dielectric stacks by LE-IBS for producing SONOS devices at low-thermal budgets, (c) design and fabrication of organic memories in collaboration with project II.1, (d) development of the PIII technique for Si-NC fabrication.

RESEARCH RESULTS

A. Block-copolymer-assisted-nanostructure fabrication for memory applications

P. Normand, K. Parisiadis, A. Avgeropoulos, P. Argitis, M. Chazichristidi, J. Raptis, G. Boulousis

The physical and technical problems associated with lithographically defining nanostructures have opened opportunities for self-assembling physical systems to play a role in preparing nanomaterials. While several self-assembly techniques (e.g. LPCVD, ion-beam-synthesis, aerosol deposition, MBE) have been tested, they fail to meet the requirements of controlled nanostructure-size, -shape, -interspacing and -density. Development of novel nanofabrication routes able to meet these requirements and their application to the production of functional nanostructures is highly desirable. Such a development constitutes the overall aim of the present task that follows a nanofabrication strategy based on block-copolymer (BC) self-assembly for nanopatterning.

BCs self-assemble into a variety of ordered structures via microphase separation. Nanostructure shapes, sizes and inter-spacing are readily tailored through the volume fraction of one of the components, macromolecular architecture, molecular weight of the different blocks and blending of the copolymer with one or more homopolymers. Proper choice of the chemical nature of the constituent blocks in combination with a variety of decomposition methods allows for the selective removal of one of the phases of the precursor material thus leading to long-range ordered nanopatterns. These nano-patterns can then be transferred to underlined substrate materials using advanced etching and deposition/growth techniques, so that nanostructures of practically any semiconductor, dielectric, metal or ferromagnetic material can be formed.

In this direction, our 2006-activities concentrated on two objectives: (1) Generation of in-plane oriented nanoscopic PMMA cylindrical domains in polystyrene materials using two asymmetric diblock copolymer P(S-b-MMA) systems. (2) Removal of the PMMA domains using selective decomposition methods for the purpose of nanoporous PS film formation. Substantial efforts were devoted on substrate preparation and diblock copolymer (DC) process parameters that can affect the size, density, orientation and ordering of the cylindrical domains. Nanoporous PS films have been successfully achieved onto Si, SiO_2 and Si_3N_4 materials.

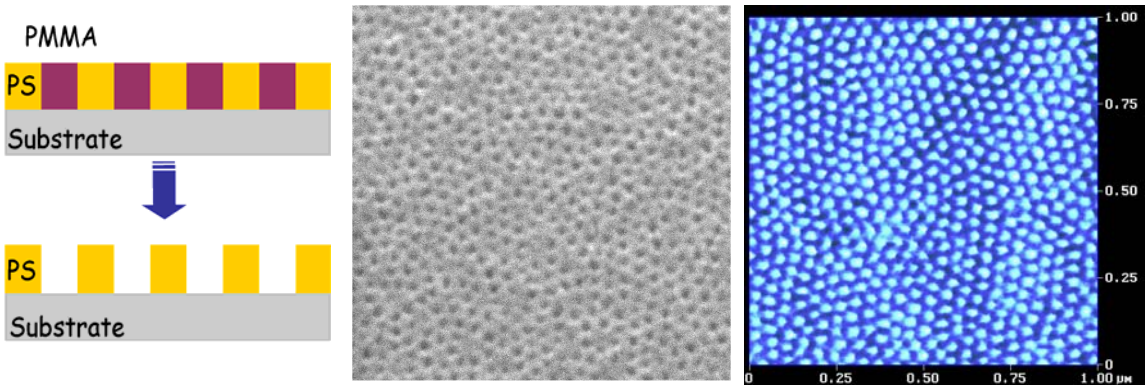

Fig. II.2.1: *Nanoporous thin film PS materials using P(S-b-MMA) diblock copolymers. (Left) Schematic describing the formation and removal of PMMA cylinders in a PS matrix. Plane-view SEM (center) and AFM (right) images of a nanoporous PS film onto Si and Si_3N_4 materials, respectively. The pores are about 20 (center) and 25nm (right) in diameter.*

B. Ge nanocrystals in high-k dielectrics obtained by low-energy ion-beam-synthesis

P. Dimitrakis, V. Ioannou-Sougleridis, P. Normand

The last few years, substantial research efforts have been placed on the fabrication of nanocrystals (NCs) in high-k dielectrics instead of SiO_2 materials to improve the performance of NC memories. Floating gate memory structures using high-k dielectrics as control and tunneling layers offer a thinner equivalent oxide thickness (EOT) without sacrificing charge retention. Band alignment of high-k dielectrics with Si results in a relatively narrow energy barrier and therefore, large tunneling currents across the tunneling layer are attainable at relatively low programming voltages. Part of our 2007-activities has been to explore the formation of Ge NCs in thin Al_2O_3 and Hf_2O layers using the low-energy ion-beam-synthesis (LE-IBS) technique and to evaluate the electrical performance of the resulting gate dielectrics.

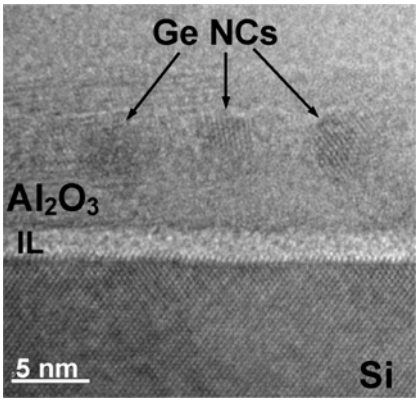

Fig. II.2.2: *High-resolution cross-section TEM image of Al_2O_3 materials with embedded Ge nanocrystals obtained by LE-IBS.*

For this purpose, 5 to 7nm thick Al_2O_3 layers were deposited on n-type Si wafers using the Atomic Layer Deposition (ALD) technique. The ALD-processed wafers were supplied by CambridgeNanotech (USA). Subsequently, the Al_2O_3 layers were implanted at FZR (Germany) with 1keV Ge atoms to doses of $5x10^{15}$ and $1.0x10^{16}cm^{-2}$. Then, a 10nm thick Al_2O_3 layer acting as control gate dielectric was deposited onto the implanted layers and the structures were thermal annealed for the purpose of Ge-NCs formation. The resulting structures were examined by transmission electron microscopy (CEMES/CNRS) and electrical characterization after fabrication of Al gate MIS capacitors.

In the case of 7nm-thick implanted-Al_2O_3 layers and thermal annealed at 800°C, high-resolution TEM (HRTEM) and Electron Energy Loss Spectroscopy (EELS) studies revealed the presence of Ge nanocrystals of 3-5 nm in diameter occupying the whole implanted Al_2O_3 layer and located at tunnel distances (1 to 5 nm) from the channel (see Fig. II.2.2). At this annealing temperature, presence of a 1nm-thick interfacial layer (IL, SiO_2-rich) between the Al_2O_3 layer and the Si substrate, as well as crystallization of the alumina matrix have been observed.

Capacitance-to-voltage characteristics of MIS capacitors with NCs revealed strong hysteresis in terms of flat-band voltage V_{fb} shift after application of gate-voltage round sweeps (see Fig. II.2.3). No significant hysteresis was detected for the unimplanted and the as-implanted samples. These results suggest that charge trapping and storage are related not only to the formation but also to the distribution of the Ge-NCs through the implanted/annealed Al_2O_3 layer. The effect of the annealing regime on the structural and electrical properties of Ge-NC-Al_2O_3 materials as well as the formation of Ge NCs into HfO_2 layers by LE-IBS are under investigation.

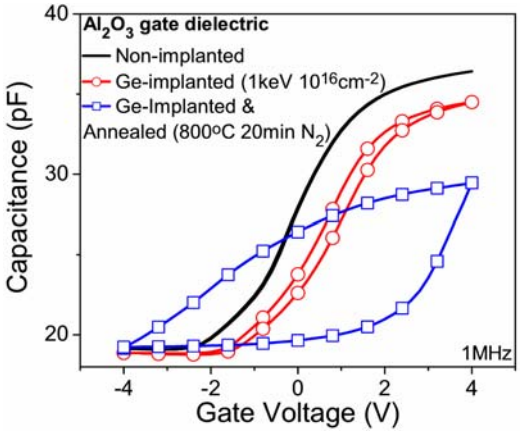

Fig. II.2.3: *High-frequency C-V curves after application of low gate voltage round sweeps.*

C. Channel edge effects in shallow-trench-isolated nanocrystal memories

P. Dimitrakis and P. Normand

Within the framework of the EU project NEON, prototype LE-IBS-Si-nanocrystal memory devices were fabricated at STMicroelectronics (IT) on 8-inch wafers using a process flow based on a 0.15μm Flash-EEPROM technology. The devices were isolated following a shallow-trench-isolation (STI) procedure. Capacitors and n-MOSFETs memory cells with gate lengths and widths ranging from 0.16 to 10 μm have been realized. Our electrical investigations stressed the following:

(a) Leakage currents occur at the channel isolation edges and lead to severe "subthreshold hump" effects in the transfer characteristics of 10x10μm2 and 0.9x0.6μm2 (WxL) devices. These leakage currents can be described in terms of parasitic transistors (FET_P) operating in parallel with the intrinsic transistor (FET_I) formed in the central part of the channel Fig.II.2.4). (b) Memory testing and threshold-voltage extraction according to the transconductance-change (TC) and constant-current methods, reveal that the parasitic transistors can be programmed or erased but exhibit memory characteristics different than that of the intrinsic transistor and thereby, can be treated as parasitic memories. Both erasing and programming are more efficient for FETI compared to FET_P. (c) No subthreshold "hump" is detected for the 0.16x0.3μm^2 devices. This is because the edge currents dominate the total drain current and the contribution of the intrinsic transistor is not immediately obvious; nevertheless the latter can be detected using the TC method (Fig. II.2.5). Further, transfer characteristics analysis and program/erase testing and comparison with capacitors and large channel area transistors reveal that the memory operation of these devices is FETP driven.

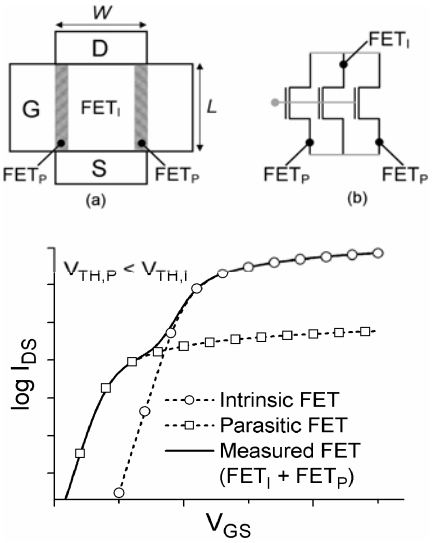

Fig. II.2.4: *Schematics describing (a) the channel edges where FET_P are formed, (b) the equivalent circuit with FET_I and FET_P, (c) the origin of the hump in the transfer characteristic of a MOSFET where FET_P are active.*

Although it is still difficult to draw safe conclusions regarding the origin of the parasitic memory effects in the devices reported here, our work suggests that the structural properties of the isolation regions affect dramatically the memory performance of the devices and may constitute a critical parameter in nanocrystal memory integration. Particular attention should be placed on STI architecture and device processing to overcome this technological concern.

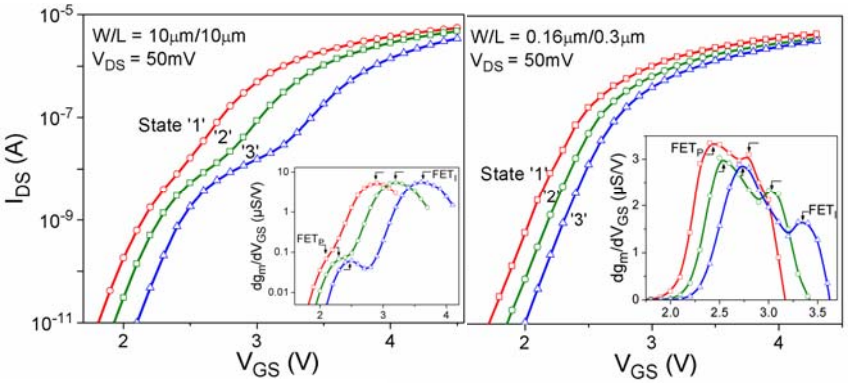

Fig. II.2.5: *Transfer characteristics of 10μm/10μm and 0.16μm/0.3μm Si-NC MOSFETs for four successive programming states. The corresponding dg_m/dV_{GS} vs V_{GS} plots are shown as insets.*

D. Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride

V. Ioannou-Sougleridis, V. Vamvakas, P. Dimitrakis, P. Normand

The use of thin tunnel SiO_2 layer (~2-3nm) in NCM technology allows high-speed operation at low voltages but addresses a critical issue for long retention times. If a thick oxide is used to enhance data retention, the advantage of high endurance and speed at reasonable voltages is lost rapidly. Different alternatives have been suggested for improving the performance of low-voltage NCMs without sacrificing charge retention. An interesting direction is to combine the advantages (low-voltage and high-speed) of NCM technology with those (long retention times, immunity to disturbance) of time-proven nitride-trap technology. Memory structures using SiO_2-Si_3N_4-SiO_2 (ONO) gate dielectric with nanocrystals embedded in the nitride layer are expected to gather together these advantages.

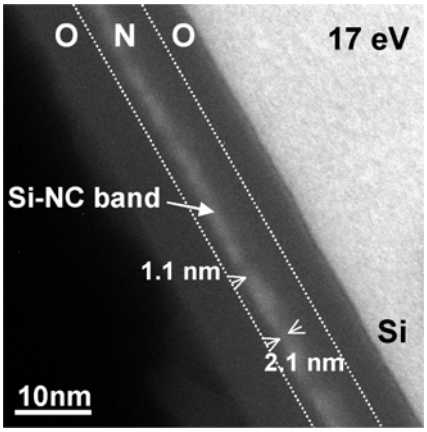

Figure II.2.6*: Cross-sectional EFTEM image (around 17eV) of a Si-NC ONO structure. The NCs were generated in the nitride layer by LE-IBS*.

Our activities in this area started in 2005 with the realization of Si-NC ONO structures where Si-NCs were generated in the nitride layer by low-energy ion-beam-synthesis (LE-IBS). SiO_2-Si_3N_4 stacks were developed onto Si substrates and subsequently implanted at CEMES/CNRS with 1keV Si ions to doses ranging from $5x10^{15}$ to $1.5x10^{16}$ cm^{-2}. The thickness of the oxide and nitride layers was 2.8nm and 6.5nm, respectively. After the steps of post-implantation annealing and SiO_2 deposition, gate electrodes were fabricated by Al evaporation and patterning. In 2006, in-depth electrical and structural investigations were conducted at IMEL and CEMES. EFTEM examination revealed the presence of Si-NC and amorphous Si nanoparticles thin bands into the nitride layer for the $1.5x10^{16}$ (see Fig. II.2.6) and $1.0x10^{16}$ Si cm^{-2} samples, respectively. Electrical measurements indicate that significant changes compared to reference ONO stacks occur in the cases of the $1.0x10^{16}$ cm^{-2} and $1.5x10^{16}$ cm^{-2} samples, such as reduction of the onset voltage for electron and hole injection, reduction in electron storage ability and establishment of hole storage. Typical memory windows attainable under pulse operation and data retention characteristics at room temperature are shown in Fig. II.2.7-8. To date, our findings suggest that the Si-NC-ONO stacks are attractive for the further development of nitride storage memory cells.

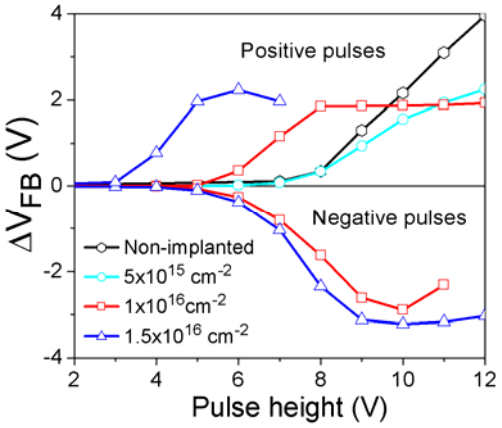

Fig. II.2.7: *Flat-band voltage shifts as a function of the gate pulse voltage of 100 ms duration for Si-implanted and unimplanted ONO stacks.*

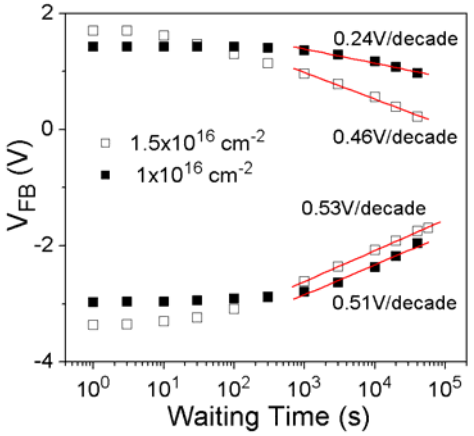

Fig. II.2.8*: Room-temperature retention characteristics of medium and high-dose Si-implanted ONO stacks.*

PROJECT OUTPUT in 2006

Publications in International Journals and Reviews

1. "Parasitic memory effects in shallow-trench-isolated nanocrystal memory devices", P. Dimitrakis and P. Normand, Solid-State Electronics, In Press, Corrected Proof, Available online 12 December 2006.
2. "Proton radiation tolerance of nanocrystal memories", E. Verrelli, I. Anastassiadis, D. Tsoukalas, M. Kokkoris, R. Vlastou, P. Dimitrakis and P. Normand, Physica E: Low-dimensional Systems and Nanostructures, In Press, Corrected Proof, Available online 16 December 2006.
3. "Metal nano-floating gate memory devices fabricated at low temperature", S. Koliopoulou, P. Dimitrakis, D. Goustouridis, P. Normand, C. Pearson, M.C. Petty, H. Radamson, D. Tsoukalas, Microelectronic Engineering 83, pp. 1563-1566 (2006).
4. "Oxidation of Si nanocrystals fabricated by ultralow-energy ion implantation in thin SiO_2 layers", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, G. Ben Assayag, A. Claverie, M. Respaud, P. Dimitrakis, P. Normand, J. Appl. Phys. 99, 044302 (2006).

Conference Presentations

1. "Self-limited oxidation of Si nanocrystals elaborated by ultra-low implantation energy ion thin SiO2 layers", C. Bonafos, S. Schamm, H. Coffin, N. Cherkashin, G. Ben Assayag, A. Claverie, P. Dimitrakis, P. Normand, V. Paillard and M. Carrada, E-MRS 2006 Spring Meeting, Symposium C, Nice, France, May 29 – June 2, 2006.
2. "Proton radiation effects on nanocrystal nonvolatile memories", E. Verrelli, I. Anastassiadis, D. Tsoukalas, M. Kokkoris, R. Vlastou, P. Dimitrakis and P. Normand, Second European Conference on Radiation and its Effects on Components and Systems (RADECS 06), Athens, Greece September 27-29, 2006.

Invited Talks

1. "Materials Science Issues for the Fabrication of Nanocrystal Memory Devices by Ultra Low Energy Ion Implantation", A. Claverie, C. Bonafos, G.B. Assayag, S. Schamm, N. Cherkashin, V. Paillard, P. Dimitrakis, E. Kapetenakis, D. Tsoukalas, T. Muller, B. Schmidt, K.H. Heinig, M. Perego, M. Fanciulli, D. Mathiot, M. Carrada, P. Normand, Second International Conference on Diffusion in Solids and Liquids, Portugal, July 2006, Material Science Forum Vol. 258-260, pp 531-541.

Ph. D. thesis

1. P. Dimitrakis, Silicon nanocrystals for electronic memory devices, National Technical University of Athens, December 2006, Supervisor: P. Normand.

Diploma Theses

1. G. Niarchos, Fabrication and testing of MOS structures for memory applications, University of Athens, September 2006, Supervisor: P. Normand.
2. K. Parisiadis, Fabrication of nanostructures using P(S-b-MMA) diblock-copolymers, University of Ioannina, July 2006, Supervisor: P. Normand.